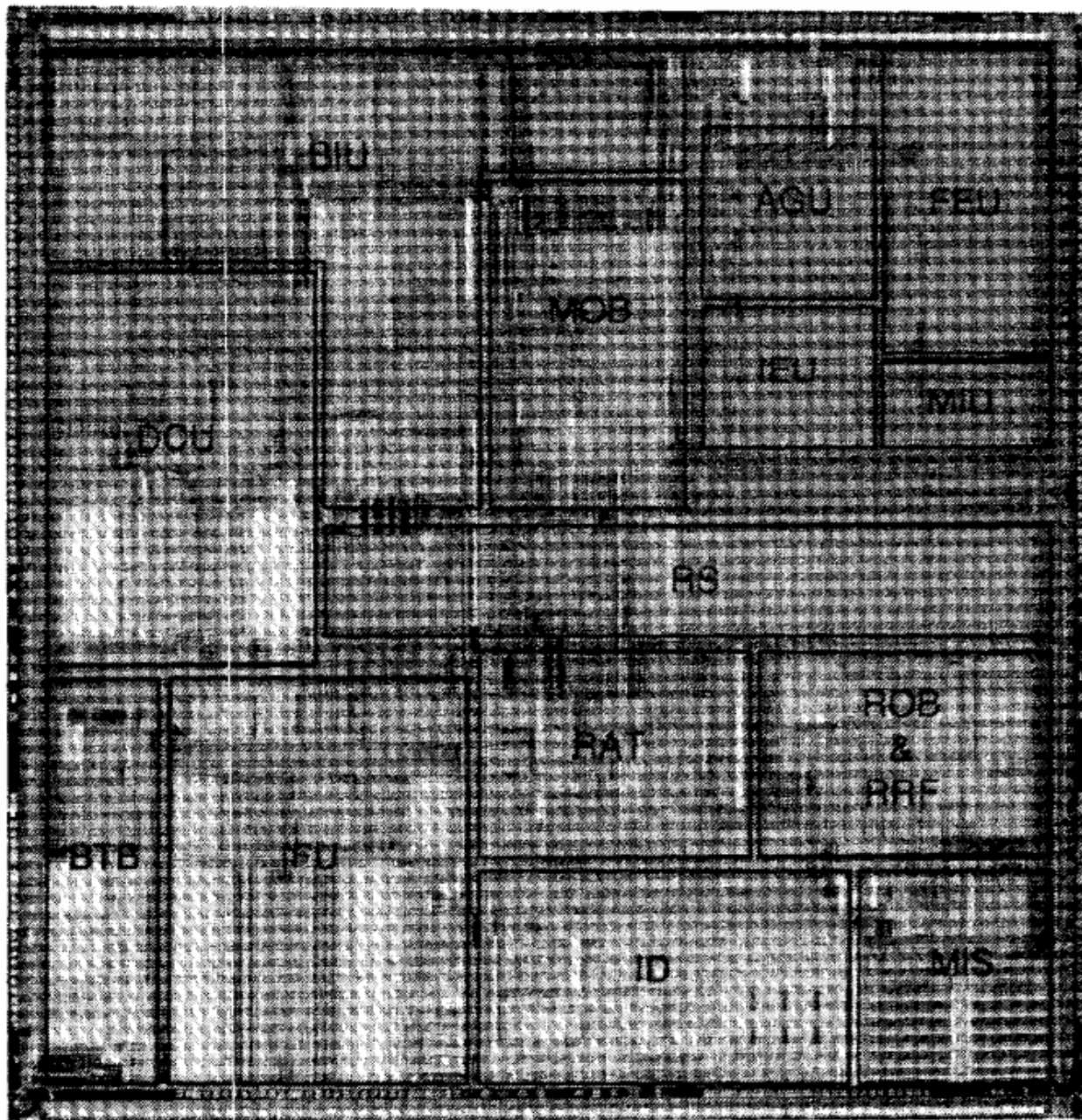


# OUT-OF-ORDER EXECUTION AND NEW ARCHITECTURAL FEATURES

*ISSCC 1995*



## **A 0.6 $\mu$ m BiCMOS Processor with Dynamic Execution**

THE PUSH TOWARDS higher performance continued with new architectural features becoming possible with the ever-increasing numbers of transistors available on-chip. In this microprocessor, parallel decoding schemes were used to break complex CISC instructions into smaller RISC-like instructions, in order to leverage the benefits of a RISC-like architecture. In addition, these instructions were executed out of order, improving performance through speculative execution. Superpipelining techniques were used to push the clock frequency higher, and these techniques became the norm across the industry as pipelines became deeper and deeper.