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IEEE Solid-State Circuits Society Quarterly Newsletter



ISSCC Focuses on Power Management

ISSCC 2003 in San Francisco, California, 9–13 February, will introduce major breakthroughs in a broad spectrum of cutting-edge wireless and portable products. The conference theme this year is “Power-aware systems.”



this
issue

<i>ISSCC Focuses on Power Management</i>	1
<i>JSSC Classic Paper: Switched Capacitor Filters Grew the Communications Industry</i>	5
<i>The Analog MOS Filter Solution</i>	5
<i>JSSC Classic Paper: The Gilbert Cell, the Linear Mixer with Gain, in CMOS or Bipolar</i>	6
<i>The Beginning of Translinear Circuit Design</i>	6
<i>The Triumph of MOS Technology: A Book Review</i>	7
<i>Five AdCom Members Elected to Serve 2003-2005</i>	8
<i>August AdCom</i>	9
<i>Beyond Brainstorming: A Book Review</i>	10
<i>Introducing Our New Chapters</i>	11
<i>Banner Year for SSCS Chapters</i>	12
<i>News from IEEE</i>	12
<i>The IEEE Solid-State Circuits Award</i>	14
<i>SSCS Events Calendar</i>	16

Power-aware design methodologies have become a major concern with the increasing use of portable multimedia and wireless devices as well as non-portable applications such as high-performance computer servers. End users continue to demand higher functionality and bandwidth, without the requirement of being attached to a fixed power source. Operating from scavenged energy and requiring extreme power management are new and exciting wireless applications using distributed sensor networks for medical monitoring and security.

System-level methodology addresses the energy efficiency of sensing, computation, and communication. Power management improvements come from modifications to the underlying process technologies, innovative mixed-signal circuits, new computation/communication architectures, and the actual improvement of energy sources.

Power-aware design methodologies are highlighted in the Plenary Sessions, in five of the nine evening sessions, in three of the four workshops, in two of the seven tutorials, the Thursday Short Course “System-On-a-Chip Design,” and in nine of the twenty-five technical paper sessions. Look for the **PA** indicator throughout this article.

Register at www.isscc.org/isscc. Articles from the Digest will be available in IEEE *Xplore*™ by early summer.

Plenary Speakers

Gordon E. Moore, Chairman Emeritus of the Intel Board, will open the Plenary Session of ISSCC Monday morning with “No exponential is forever: but ‘forever’ can be delayed!” Musing that the number of transistors produced each year has grown by eight orders of magnitude in thirty years, Moore will review how the law named after him has been applied to many metrics in the semiconductor industry, such as processor clock performance, number of transistors on a die, and world-wide revenue. However, several

issues can limit this exponential growth, including processor power dissipation, integration complexity and verification, and complexity and cost of emerging device structures. At least another decade of device, circuit, and architecture innovations will continue exponential growth. **PA**

Takayasu Sakurai, University of Tokyo, will focus on one of these limits with “Perspectives on power-aware electronics.” Device leakage is dramatically increasing with technology scaling. Innovative leakage mitigation techniques will be required to achieve long system battery lifetime, and energy efficiency is a critical metric in battery-operated and “self-powered” electronic systems. To address the power problem, Sakurai takes a systems view that requires cooperation between circuit/device techniques and system software. **PA**



Five New AdCom Members See Page 8

Evening Special Topic Sessions

Sunday

- Highlights of DAC
- Circuits for Emerging Technologies ^{PA}
- How Far Can Integration Go for 3G Cell Phones? ^{PA}

Monday

- Analog IP – Stairway to SOC Heaven?
- Will MEMS, Imagers, and Displays Be Key to the Growth of the IC Industry? ^{PA}
- Good, Bad, Ugly – 50 Years of Memory Evolution. What Next?

Tuesday

- Future Mobile Phones: A Beautiful Dream or Smoke in LSI Technology? ^{PA}
- Finline Prototyping: Breaking New Ground or Breaking the Bank?
- SOC: DOA? RIP? ^{PA}

Bruno Murari, STMicroelectronics, Cornaredo, Italy, will present “Interfacing electronic systems to the external world.” While there has been a huge increase in the computing power of digital circuits, there has not been a similar evolution in circuits that interface to the external world. Murari holds that low-voltage CMOS is inadequate for interface applications, and emphasis must be placed on BiCMOS, HVC MOS, and BCD. System-On-a-Chip and System-In-a-Package technologies will enable integration of MEMS and photonic technologies with conventional electronics.

Evening Special Topic Sessions

Evening Special Topic Sessions provide a range of treats primarily for the benefit of attendees, as they are not documented in the conference Digest.

Starting before the traditional weekday opening, Sunday evening will have three sessions. The first will highlight four prime technical presentations from the Design Automation Conference. At the second Ian Young, Intel, will chair “Circuits for emerging technologies,” featuring a range of five specific circuit techniques for high-performance microwave frequencies and giga-scale ICs that may emerge as the right match with fabrication process technology. Finally Trudy Seltzer, TI, will chair “Integration for 3G Cell Phones,” which features four speakers on trends and tradeoffs in baseband and RF sections of the 3G system.

Weeknight Evening Special Topic Sessions will tend toward the more freewheeling controversy-based panels on a specific application or challenge. Half a dozen experts will volley back and forth with a moderator keeping the ball in play.

Analog

Monday afternoon’s Session 3 on oversampled converters will feature a number of “continuous time” modulators that set new records for low power at high performance. It also provides the first “triple mode” modulator for cellular phones, presented by R. van Veldhoven, Philips Research, Eindhoven, The Netherlands.

Tuesday morning’s Session 7 on DACs and AMPs will provide a variety of analog and mixed-signal circuits pushing dynamic range and speed. W. Schofield et al., Analog Devices, will demonstrate a 16-bit DAC producing high-dynamic range signals at 300 MHz output frequency. This is a major advance for signal generation with linearity sufficient for upcoming wireless applications, at –80 dBc intermodulation distortion.

Wednesday morning’s Session 18 on Nyquist ADCs will open with a CMOS circuit by K. Poulton et al., Agilent Laboratories and Agilent Technologies, that pushes the parallel pipeline out to the “lunatic fringe,” sampling at 20 GS/s with an 8-bit resolution.

Wednesday afternoon’s Session 23, “Mixed-signal and wireline technologies,” will present an unusual very-low-power technique. S. Ran-

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ganathan and Y. Tsvividis, Columbia University demonstrate that a voltage sampled on the gate rises when the channel charge is pulled out. By varying the operating region of a MOSFET, its small-signal capacitance changes. Based on the 40-year-old idea of the parametric amplifier, noise-free amplification is implemented.

ISSCC 2002 Schedule of Session Topics

	Monday afternoon	Tuesday morning	Tuesday afternoon	Wednesday morning	Wednesday afternoon
Analog	3	7		18	23
Digital	6		14	19	24
Imagers, Displays, and MEMS		11	12		
Memory			16	17	26
Signal Processing	2	8			
Technology Directions		9		21	22
Wireless Communications	5		15	20	25
Wireline Communications	4	10	13		23

Digital

Session 6 on Monday afternoon will focus on the conference theme of power aware systems. J. Tschanz et al., Intel, will present a multifaceted approach to controlling transistor leakage power for an integer ALU. Using sleep transistors, active body biasing, and conventional clock gating, this work studies the idle time required to achieve power savings. A minimum required idle time is reported that is needed to reduce leakage during the idle periods and increase the performance of the part during active periods.^{PA}

Session 14 on Tuesday afternoon will present continued advances in microprocessor integration and computation power, resulting in chips with over 400 million transistors and processor components operating at 5 GHz. H. Ando et al., Fujitsu, will introduce the 1.3-GHz 35-W SPARC64 built with 130-nm CMOS process and eight layers of Cu metallization. J. Stinson and S. Rusu, Intel, will introduce a third generation 64-bit Itanium processor, operating at 1.5 GHz.^{PA}

Clocking circuit design in microprocessors show notable advances in two sessions. N. Bindal et al., Intel, will present a multi-GHz processor-clock of three-level distribution design for the next generation of Pentium processors, with less than 10 picoseconds of skew, on Wednesday morning in Session 19. On Wednesday afternoon in Session 24, R. O'Mahony et al., Stanford University and Atheros Communications, will present a novel prototype concept, a 10-GHz clock distribution with less than 1 picosecond of skew using coupled standing-wave oscillators.

Imagers, Displays, and MEMS

Wednesday morning's Session 11 will feature a number of advances for the biomedical industry. N. Manaresi et al., Silicon Biosystems and University of Bologna, Italy, will present a CMOS chip that detects and manipulates more than 10,000 individual cells in parallel, useful for investigating cell interactions for drug screening, cell separation, and cell analysis. Later in the same session, M. Xue et al., Hong Kong University of Technology and South East University, Nanking, China, will present a CMOS chip for DNA identification.

Wednesday afternoon's Session 12 will feature CMOS chips that embed analog and digital circuitry to collect "raw images" and extract information about fingerprints, neural signals, computational vision, and projection. I. Takayanagi et al., Micron Imaging, Tokyo, will introduce a large-format video camera chip, an 8.3 mega pixel sensor in CMOS that provides images for ultra-high-definition television while consuming only 760 mW.

Memory

Memory papers will present breakthroughs in nonvolatile memories. In session 16, M. Crowley et al., Matrix Semiconductor, Santa Clara, California, will open a new era in 3D memory architecture, fabricating eight layers of memory planes above CMOS peripheral circuits, lowering cost. Only a small percentage of the chip area (relative to other non-volatile memories) is devoted to memory-cell construction. J. Lee et al., Samsung, Republic of Korea, break records with the smallest yet NAND

Flash cell, reporting for the first time the use of 90-nm technology to produce 2 Gb of Flash storage. With its low 1.8-V operation this technology expands new portable mass-storage applications.

Signal Processing

Monday afternoon's Session 2, "New levels of integration for DVD processors," will demonstrate that System-On-a-Chip

designs are poised to play key roles in effective solutions that meet cost, performance, and power constraints for real-time digital video and audio for the consumer market. K. Okamoto et al., Matsushita, embeds most of the building blocks for a complete DVD player on a 64-mm² die using only 1.5 W. A DVD decoder directly reads the data channel and then interfaces directly to the video display and the audio output channel. J. Geerlings et al., Phillips Semiconductors, will present an integrated MPEG-2 video and audio encoder/decoder that supports DVD+RW and digital video recording applications.^{PA}

In Session 8 on Tuesday morning, D. Carlson et al., Cavium Networks, Santa Clara, California, will present a security processor that provides the most integrated and fastest SSL handshake available. Secure internet connections are established via security protocols such as Secure Socket Layer (SSL) and Internet Protocol Security (IPSEC). Later in the same session, several power-efficient Turbo decoders will be presented for improved 3G wireless devices to deliver high-speed data services via mobile cellular networks.^{PA}

Technology Directions

Session 9 on Tuesday morning will present technologies, systems, and architectures for advanced computer designs, smart PDAs, and digital cinematography, each integrating extremely complex systems onto a single device. Hugo De Man et al., IMEC, Leuven, Belgium, and Alcatel, Antwerp, Belgium, will discuss design methods to bridge the high-level system/software abstractions of these

complex systems and the physical and electrical models of the chips.

Session 21 on Wednesday morning will showcase the new organic technologies that offer the potential of new and ultra-low-cost applications, as well as advances in silicon technology and devices. For example, E. Huitema et al., Philips Research, Eindhoven, The Netherlands, will demonstrate a display using plastic transistors with potential for future flexible displays.

Session 22 on Wednesday afternoon will present key technologies to embed for portable systems; power generation and power optimization technologies; as well as on-chip and wireless communications technologies. Two thermogenerators will be presented that convert body heat into electricity by finding or creating temperature difference. S. Jung et al., Infineon Research, Munich, Germany, will describe several technologies needed in the area of wearable electronics, such as chips and antennas woven into "smart clothing" with copper replacing fabric threads and again harvesting energy from body heat. T. Douseki et al., NTT, Atsugi, Japan and Seiko, Japan, will present a 100- μ m thick RFID tag chip with front and backside contacts for attachment to a dipole antenna; the tag chip can be fabricated on paper or fabric media for wearing. M. Schmidt of MIT, Cambridge, Massachusetts, will describe two MEMS-based devices that burn fuel to generate power as an alternative to conventional batteries. PA

Wireless Communications

Session 5, "Wireless PAN transceivers," on Monday afternoon will feature several outstanding presentations in the areas of Bluetooth/802.11b integrated transceivers, and performance and cost improvements for standalone Bluetooth solutions. The first published 802.15.4 radio also will be presented by P. Choi et al., KAIST Daejeon, Republic of Korea. PA

Presentations on cellular communications are scheduled for Session 15 on Tuesday afternoon. New circuits for WCDMA transceivers implementing direct conversion will be presented. This session also features a fully integrated direct conversion GSM-GPRS transceiver that provides GSM850/GSM/DCS/PCS functionality, authored by E. Duvivier, Texas Instruments, Villeneuve Loubet, France. PA

The initial adoption of Wireless Local Area Networking (WLAN) technology has been sluggish. However, the recent demand in wireless networking in public hot spots, enterprise networking, and home networking, together with advances in IC technology enabling lower-cost integrated solutions, have provided significant growth in the last couple of years. Session 20 on Wednesday morning will present a number of different solutions for 802.11a and 802.11b transceivers, as well as building blocks for future developments in the wireless area. PA

The RF Infotainment Session 25 on Wednesday afternoon will demonstrate several RFICs that are enabling new classes of entertainment and information appliances. This session will feature several presentations on integrated solutions for satellite,

cable, and terrestrial tuners. The session also will present a SiGe BiCMOS up-converter for cable head-end applications for Video-on-Demand systems, as well as several building blocks for future systems by K. Ashby et al., Microtune, Plano, Texas. PA

Wireline Communications

Monday afternoon's Session 4, "Clock recovery and backplane transceivers," will feature several advances in 3- to 10-Gb/s copper-link signaling. Numerous high-density PC-motherboards and router backplanes will be presented as well as high-speed inter-chip communications.

Tuesday morning's Session 10, "High-speed building blocks," will cover a wide range of topics on high-speed data transmission. H. Wu et al., Cal Tech, Pasadena, California, and IBM Thomas J. Watson Research Center, cut the cost of both SONET and 10-Gb Ethernet by using a CMOS analog transversal filter to extend transmission distances on multi-mode fibers. S. Gala and B. Razavi, UCLA, present one of two papers comparing different 10-Gb/s laser drivers; they fabricated a 10-Gb/s limiting amplifier and laser driver chip in 180-nm CMOS.

Tuesday afternoon's Session 13, "Communicating at 40 Gb/s," will describe the first ICs to meet the high-level industry standard for optical systems. 40-Gb/s circuits are a reality in several technologies like SiGe, CMOS, and InP. The first complete chipsets for OC-768 and SFI-5 standards systems are moving into mainstream technologies like SiGe.

More for Registrants

A special event for registrants to enjoy at their leisure this year will be full-length video interviews with five ISSCC pioneers, available on one of the Marriott Hotel in-room TV channels. The interviews are part of the 50th anniversary of the ISSCC, which was first held in 1954. Interviewed were pioneers involved in the initial formation of ISSCC: Richard Baker (MIT Lincoln Labs), Murlin Corrington (RCA), John Linvill (Bell Laboratories), Arthur Stern (General Electric), and Jerry Suran (General Electric). ●

Workshops, Tutorials, and Short Courses

Sunday Workshops

Analog Telecom and Circuit Concepts
SSCTC Workshop: Implications of Near-Limit CMOS on Circuits and Applications PA

Sunday Tutorials

Attendees may register for a maximum of three tutorials. Taught by experts from the Program Committee, these 90-minute sessions are aimed at meeting attendees' needs for introductory material in the respective topics. These sessions fill up fast.

Basics of Serial Backplane Transceivers

Design for Test and Debug
Introduction to BioMEMS
MRAM: Technology and Circuits
Wireless LAN: Architectures and Design PA
Highly Integrated RF and Wireless Transceivers PA
DSL Splitters and Drivers

Thursday Short Course

System-On-a-Chip Design PA

Thursday Workshops

Microprocessor Design in the Power-Constrained Era PA
Gigahertz Radio Front Ends PA

A JSSC Classic Paper:

Switched Capacitor Filters Grew the Communications Industry

Filtering circuits, the most ubiquitous of electronic signal-processing functions, made for spirited discussions as analog-to-digital technology solutions unfolded. Bedrich Hosticka's 1978 paper on a MOS switched-capacitor filter marked the beginning of the dominance of switched-capacitor techniques for integrated audio-band filtering. In the ISSCC 40th Anniversary Commemorative Supplement in 1993, Robert W. Brodersen remembered that in the year following Hosticka's paper two papers at ISSCC 1979 demonstrated the manufacturability of the approach in high-volume applications. The circuit served as part of an icon of the era of IC telecom, when a chip plot of 30 poles of switched-capacitor filtering by B.J. White, G. M. Jacobs, and G.F.Landsburg hung in the New York Museum of Modern Art for a number of years.

Published in the December 1977 JSSC, "MOS-sampled data recursive filters using switched-capacitor integrators" by Bedrich Hosticka, Robert Brodersen, and Paul Gray, University of California, Berkeley, California, is the fourth most frequently cited article ever published in the JSSC. It has been cited more than 150 times according the Journal Citation Report 2000 Science Edition. The concepts were presented first in February of the same year at ISSCC.

Unknown to Hosticka and his coauthors in 1978, James Clerk Maxwell had explained the equivalence of a periodically switched capacitor to a resistor in *A Treatise on Electricity and Magnetism*, Oxford, The Clarendon Press, pp. 420-421, 1892. The opportunity for practical realization of filters came only with the development a zero-offset electronic switch and an infinite input impedance electronic amplifier. The MOS transistor was the first device to meet both requirements, 80 years later. Professor Yannis Tsididis at Columbia found this early prior art.

Prof. David Hodges of UC Berkeley, a co-recipient of the 1983 IEEE Morris Liebmann Technical Field Award for switched capacitor filters, notes: "SC filters found effective use only below 1 MHz analog. In that range, due to the progress in digital technology, digital filters used with delta-sigma A/D converters have almost entirely superseded SC filters for high-order functions.

Switched-C filters still are used for simple filter functions that can't justify the overhead associated with DSP filters, e.g. some toys. L-C filters still are used for very simple filters, such as the signal splitter that separates the DSL channel from the voice/fax channel on a home telephone line - excellent surge immunity, zero power consumption!"

As so frequently happens in the industry, a new technology emerged, had major impact, and then was superseded by subsequent advances and requirements.

The original paper is available on the Solid-State Circuits Digital Archive 2002 DVD. See page 13. (IEEE product # JD3755B)

The Analog MOS Filter Solution

The paper was a result of my PhD thesis research from 1974 to 1977. When I started my work at the Department of Electrical Engineering and Computer Science of the University of California, Berkeley, nobody believed that you could realize analog integrated circuits using MOS technologies (actually, all analog integrated circuits realized at that time were using bipolar technologies). It was the Department of EECS in Berkeley that pioneered the analog MOS (and later CMOS) design. This work was carried out by a group guided by Berkeley professors Paul R. Gray, R. W. Brodersen, and David A. Hodges. They created an environment that attracted gifted young engineers

from all over the world who generated a number of new ideas. It was this work that laid down the foundations of analog CMOS design.

I was among the first PhD students who joined the group. My work, inspired mainly by Paul Gray and R.W. Brodersen, introduced a new analog circuit design technique, which we called "switched-capacitor" technique. Based on novel analog switched-capacitor filters, we showed that analog switched-capacitor circuits not only "work" but also deliver excellent performance. The summary of the work appeared in the December 1977 issue of the *IEEE Journal of Solid-State Circuits*. I believe that this paper helped start a revolution

in integrated circuit design, the consequences of which we feel to this very day.

I was glad to be present at the birth of an invention—and to contribute a little bit. I learned a lot from my professors (to whom I owe very much) and I have gained many friends as well—my thanks goes to all of them. ●



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A JSSC Classic Paper:

The Gilbert Cell, the Linear Mixer with Gain, in CMOS or Bipolar

The Gilbert cell, initially designed with bipolar transistors to operate as a precision multiplier, is widely used in modern communication systems as a mixer and frequency translator. The Gilbert cell offers advantages such as high conversion gain and high port-to-port isolation. Its principle of operation is technology independent and can be realized in bipolar or CMOS processes. Because of their low fabrication costs, Gilbert cells are appropriate for high-level integration and realize good high-frequency performance. Manolis T. Terrovitis and Robert G. Meyer summarized these traits that make the Gilbert cell so popular in recent papers in the June 1999 and October 2000 *JSSC*.

Barrie Gilbert first introduced "A precise four-quadrant multiplier with subnanosecond response" at the 1968 ISSCC. Donald O. Pederson and James E. Solomon, editors of the December *JSSC* issue where Gilbert's full paper first appeared, noted "Linear IC applications are undergoing tremendous growth due largely to the development and acceptance of the integrated operational amplifier." They also noted that "the twenty-five cent IC no longer seems a remote possibility."

In the December 1982 *JSSC*, David C. Soo and Robert G. Meyer first reported NMOS fabrication of the multiplier with performance adequate for signal processing and linearity comparable to bipolar circuits in "A four-quadrant NMOS analog multiplier." Soo and Meyer recommended these applications of the multiplier circuit; automatic gain control, waveform generation, modulation, demodulation, and frequency translation. Analog MOS large-scale integrated circuits had been demonstrated as early as 1978 by D. A. Hodges, P.R. Gray, and R.W. Broderson in "Potential of MOS technologies for analog integrated circuits," published in the June 1978 *JSSC*.

Since its appearance, Gilbert's 1968 paper has become the fifth most frequently cited paper from the *JSSC* and the earliest *JSSC* paper to be cited over 100 times. The original paper is available on the *Solid-State Circuits Digital Archive 2002 DVD*. See page 13. (IEEE product # JD3755B).

The Beginning of Translinear Circuit Design

In the autumn of 1954, I met my lifetime companion and partner, whom we'll identify just by the initials "BJT," at a research lab in the south of England. After a decade of deepening familiarity and joyous discovery together, we moved to Oregon, to continue our adventures at Tektronix. This company, dedicated to fashioning the world's finest oscilloscopes, took the unusual step in 1965 of establishing an integrated circuit production line, to support future instrumentation.

Although the wafers were only one inch in diameter, this "move to monolithic" was to herald a new life for BJT, and was unquestionably the most significant milestone in my life. This was a time of charming naiveté, long before microprocessors and memories made an appearance. IC masks were generated by taking an Exacto knife to "Rubies" and cutting them practically straight from hand-drawn, slide-rule-designed schematics. SPICE was brewing in Berkeley, but not quite ready for serving.

At Tektronix, my job was to design the new 7000-series oscilloscope, using custom ICs to address

the growing sophistication and bandwidth of these instruments. However, I had enormous latitude to experiment in this new medium, which allowed me to develop many interesting and curious circuit cells. Equally exciting were novel semiconductor devices exploiting "super-integration." Unlike conventional node-by-node circuit development, where the physical extent of a transistor had no fundamental bearing on the function, these structures exploited the juxtaposition of numerous transistor fragments—bits of NPNs and lateral PNP's—to elicit specific and practically useful functions, both analog and logical. I²L was one later development of these ideas.

Meanwhile, analog design was taking the first tentative steps to explore new possibilities presented by the unique properties of monolithic fabrication, namely: (1) the close matching and (2) isothermal operation of (3) many essentially identical BJTs. Design in this medium was still in its infancy. Only a handful of basic cells were widely known and used. Two youngsters were especially promising: the differential pair and the cur-

rent mirror. An inevitable coalition was only steps away.

Each of these cells comprised only two transistors. But what a wealth of possibilities they afforded! How predictable their mathematics, over huge spans of collector current! What made the "diff pair" so intriguing was the possibility of using it as an analog multiplier by applying a voltage-mode signal across its base nodes and varying the "tail" current (the common emitter bias) to alter the magnitude of the differential collector current. As it happened, the 7000-series needed such a multiplier to provide a variable gain function in circuitry buried deep in the system, which could be controlled at a distant location (the front panel). Its bandwidth needed to extend from DC to several hundred megahertz.

The diff pair multiplier was well-suited to this challenge, except for one problem: the linearity of the transconductance from the base nodes to the output was poor (the nonlinear TANH function). On the other hand, the current mirror was basically a pure current-mode circuit with good linearity over a huge range

of currents; and, as a signal processing element, it exhibited a bandwidth close to the f_T of the transistors, which, in Tek's first-generation process, peaked at about 600 MHz.

So, the stage was set, but the plot began with a question: How could the variable-gain aspect of the diff pair be combined with the linearity of the current mirror? The felicitous answer sprang, as is so often the case, by toying with "What If?"—the most potent path to invention.

What if we placed two current mirrors side-by-side, with their output-side transistors facing inward, and all the emitters grounded? In this topology, their functions are completely independent. Now, what if we take that Exacto knife

and cut loose the lines to the two inner emitters from their ground ties? What happens if we then rejoin these two emitters at an independent node? The inner transistors have just become a simple differential pair, but driven now from the difference voltage across the outer, diode-connected transistors of the remaining fragments of the mirrors. What if we now provide a variable current to that new center node, to bias this fledgling diff pair? Bingo.

When the excitement of discovery had abated, and pencil was placed more thoughtfully to paper, it transpired that, with this simple bit of do-it-yourself surgery, the four transistors had suddenly become something radically different. We had a new entity: a purely

current-mode multiplier cell that operates in two-quadrants of the algebraic plane. Adding a second similarly biased diff pair, their bases driven in parallel with the first, but whose collectors are cross-connected to the output, created the four-quadrant sub-nanosecond multiplier described in the paper.

That was only the beginning of translinear circuit design, which quickly blossomed into dozens of fundamentally new cells, and which continues to bear fresh fruit to this day. ●



Barrie Gilbert
Analog Devices

The Triumph of MOS Technology: A Book Review

To the Digital Age: Research Labs, Start-Up Companies, and the Rise of MOS Technology by Ross Knox Bassett, published by Johns Hopkins University Press, 2002. ISBN 0-8018-6809-2

Ross Bassett's book almost could have been written as a novel titled "The Triumph of MOS Technology." Its exciting plot and cast of characters led to the current explosion of electronics in the world.

The book takes us from the invention of the bipolar transistor (invented after the fundamental unipolar surface device, for which no suitable technology existed) to the MOS structure that has made today's technology possible. Bassett tells the story of how Fairchild seeded Silicon Valley with start-ups; some successful and others not. He describes the environment in which knowledge was shared across company boundaries and reviews the incredible mobility of developments throughout the valley. If a new process was needed by company A, it could be acquired very easily by hiring an engineer (who had already developed the process) from company B. If a potential

product looked promising but was not being pursued with the enough vigor in the eyes of the originator, a new company would be formed that would give it the attention it deserved. Bassett identifies four such start-ups by Fairchild people between 1959 and 1962. By 1968

"A fascinating account of a critical period in the evolution of microelectronics. The author clearly documents the cost of 'not invented here' attitudes, and the importance of close coupling between R&D, manufacturing, and marketing in fast-changing fields."

D. A. Hodges, University of California at Berkeley

Fairchild's dominance in the semiconductor vendor market had ended. In 1968 there were twelve new start-ups, one of which was Intel, and there were an additional nine start-ups in 1969.

One of the dominant figures in the spread of the MOS gospel was Frank Wanlass, inventor of the now-ubiquitous CMOS circuit and a very itinerant practitioner. Bassett tells the story of Lee Boysel, a disciple of Wanlass. While working for IBM in Hunstville, Boysel approached Wanlass (who was at General Instruments) to get a MOS chip designed and built. Boysel ended up working with Wanlass to complete the job. Eventually, Boysel (who had moved to Fairchild) took several members of his MOS design group from Fairchild and started his own company. Such interactions and defections were common in the early days of Silicon Valley. The raiding of the enormous amount of talent assembled at Fairchild and the creation of a boundaryless pseudo-company that became known as Silicon Valley is probably unique in the development of a new technology: intellectual property was disseminated by the movement of people and the free flow of information in technical conferences and scientific publications.

continued on page 10

Five AdCom Members Elected to Serve 2003–2005

The SSCS membership elected three new and two returning AdCom members in the Fall 2003 election: Anantha Chandrakasan, John Corcoran, Wanda Gass, Teresa Meng, and Jan Sevenhans. Their term of office begins on 1 January, 2003 and continues for three years.

We wish the newly elected AdCom members success and thank all candidates for their willingness to serve and for permitting their names to be included on the ballot. Our society and profession benefit from their dedication, expertise, and time.

Anantha P. Chandrakasan is reelected to a second term on Adcom. He received his PhD degree in EECS from the University of California, Berkeley, in 1994. He has been at MIT since 1994 and is currently an associate professor of EECS. He held the Analog Devices Career Development Chair from 1994 to 1997. He received career development awards from NSF, IBM, and National Semiconductor. He is a co-founder and Chief Scientist at Engim, a company focused on high-performance wireless communications. His publication awards include the 1993 IEEE Communications Society's Best Tutorial Paper Award, the IEEE Electron Devices Society's 1997 Paul Rappaport Award for the Best Paper in an EDS publication, and the 1999 Design Contest Award from DAC.



His research interests include the low-power implementation of integrated systems, wireless microsensors, and emerging technologies. He is a co-author of "Low-Power Digital CMOS Design" and a co-editor of "Low-Power CMOS Design" and "High-Performance Microprocessor Circuits."

He has served on the program committee of various conferences including ISSCC, VLSI Circuits Symposium, DAC, ESSCIRC, and ISLPED. He has served as a techni-

cal program co-chair for ISLPED '97, VLSI Design '98, and SiPS '98. He served as an associate editor for the IEEE *JSSC* from 1998 to 2001. He was the technical program vice-chair for ISSCC 2002 and is the technical program chair for ISSCC 2003.

John J. Corcoran is reelected to a second term on Adcom. He received his BS degree in electrical engineering from the University of Iowa in 1968 and his MS degree in electrical engineering from Stanford University in 1970. From 1969 to 1999 he was with Hewlett-Packard Company, first at the Santa Clara Instrument Division, then at Hewlett-Packard Laboratories in Palo Alto, California. His work at HP focused on integrated circuit design in bipolar, CMOS, BiCMOS, CCD, GaAs MESFET, and GaAs HBT technologies. He is presently manager of the Mixed-Signal Electronics Department at Agilent Laboratories, which develops integrated circuits for instrumentation and communication applications. He has published numerous papers on high-speed A/D conversion and A/D testing, and was co-author of the paper "A 1-GHz 6-bit ADC system," which received the Best Paper Award from the IEEE *Journal of Solid-State Circuits* for 1987–1988. He received the Best Evening Panel Award from the 1988 International Solid-State Circuits Conference (ISSCC) and the Beatrice Winner Award for Editorial Excellence from ISSCC in 1992. He has served as Guest Editor for the IEEE *Journal of Solid-State Circuits*, and from 1994 to 1997 and was Secretary to the IEEE Solid-State Circuits Council. He was named a Fellow of the IEEE in 2001.



Wanda Gass received her BSEE degree in 1978 from Rice University and her MS in Biomedical Engineer-

ing from Duke University in 1980. She has been with Texas Instruments since 1980 where she is a TI Fellow. She was a key contributor in the development of the first programmable DSP at TI, for which she has been granted three critical patents. During her career she has done work in VLSI design, software for speech codecs, multiprocessor system design for speech recognition and image processing, silicon compilers for DSP functions, video compression hardware design, GSM systems, and W-CDMA hardware and software implementations. Currently she defines the instruction set architecture and low-power strategy for high-performance DSP processors.



Ms. Gass is a Senior Member of IEEE. She is an active member in the Signal Processing Society and the Solid-State Circuits Society. In the SSCS she has served as Member (1995–1999) and Chair (2000–2002), ISSCC Technical Committee, Signal Processing Sub-committee (1995–1999). In the SPS she has served as Member (1990–1996) and Chair (1997–1999), Design and Implementation of Signal Processing Systems Technical Committee. She was instrumental in facilitating the Signal Processing System Workshops from 1997 to 2002. She has also served as editor for the *Journal of VLSI Signal Processing* (Kluwer Academic).

Teresa H. Meng received her PhD in EECS from the University of California, Berkeley, in 1988. She joined the faculty of the Electrical Engineering Department at Stanford University in 1988, where she is now a professor and the Robert Bosch Faculty Fellow. Awards and honors for her research work at Stanford include an NSF Presidential Young Investi-



gator Award, an ONR Young Investigator Award, an IBM Faculty Development Award, a best paper award from the IEEE Signal Processing Society, the Eli Jury Award from U.C. Berkeley, and awards from AT&T, TRW, and other industry and academic organizations.

In 1998, Dr. Meng took leave from Stanford and founded Atheros Communications Inc., which provides the core technology for ubiquitous, high-performance wireless communications. Dr. Meng was named one of the Top 10 Entrepreneurs by Red Herring in 2001, and Innovator of the Year by MIT Sloan School of BA in 2002. She returned to Stanford in 2000 to continue her research and teaching at the University.

Dr. Meng's current research activities include high-frequency linear PA design, wide-band wireless architectures, and bio-signal processing circuits. She has given many plenary talks at major con-

ferences in the areas of signal processing and wireless communications. She is the author of one book, numerous book chapters, and over 200 technical articles in journals and conferences. Dr. Meng is a Fellow of the IEEE.

Jan Sevenhans is a Distinguished Member of the Technical Academy of Alcatel Bell in Antwerpen, Belgium, and an IEEE Fellow recognized for "contributions to solid-state telecom transceiver integration."



He serves as European Chair of the International Solid-State Circuit Conference (ISSCC) held each February in San Francisco. In 2002 he chaired the workshop "Analog telecom access circuits and concepts" held in conjunction with the ISSCC.

He was born in 1955 and completed his Masters in 1979 at the KULeuven in Belgium. His PhD in 1984 at the same university focused on the subject of CCD imagers for facsimile applications. Since 1987 he has worked at Alcatel Bell on analog and RF circuit design for telecom applications in GSM, ADSL, ISDN, POTs, and on CMOS and bipolar silicon technology. He has filed many patents and published many articles in IEEE conferences and journals.

Since the late eighties he has been involved with many European research projects on GSM in Jessi, Medea, Medea+, RACE, IST, and ESPRIT, for example Girafe — Gigahertz Radio Front Ends, in addition to Medea A203, SODERA, and SPACE. He also acted as reviewer and/or evaluator of several European projects over the past ten years. ●

August AdCom

The SSCS AdCom met 26 August 2002 in San Francisco, California. Much of the action supported chapters and conferences. Applications for subsidies for 19 chapters, totaling \$16,000 were approved. Loans were approved for fully sponsored Society meetings, the Custom Integrated Circuits Confer-

ence in the fall, the Symposium on VLSI Circuits in June, and the Solid-State Circuits Technology Committee Workshops held twice a year (in February and the fall). Technical cosponsorship was approved for ESSCIRC, BCTM, and GaAsIC. Bryan Ackland was appointed as an official SSCS representative to DAC. Email distrib-

ution of the Society newsletter was approved. See the details about the launching of this new program on the back page.

The five candidates recently elected to AdCom will meet with the full AdCom on Sunday, 9 August, prior to the opening of ISSCC. ●

Congratulations to New SSCS Senior Members

Edwin de Angel
Salvador R. Bernadas
Werner Bonath
George Z N Cai
Jules D. Campbell, Jr.
Michael Ciraula
Uday Dasgupta
Kobchai Dejhan
Ahmad B. Dowlatabadi
ChoonNgia Ho
Werner Hoelzl
Tian-Wei Huang
Ronald B. Hulfachor
Hajime Ishikawa

Sumant K. Katiyal
Darwin L. Jallice
Xiukuan Jing
Peter Maurice Lee
Phillip H.W. Leong
Howard C. Luong
Vijayakumaran Nair
Tadao Nakagawa
Shedrach S.N. Okeke
Jeffrey J. Peterson
Martin O. Rieger
Timothy T. Rueger
Michael R. Seningen
Ali Sheikholeslami

Joseph S. Shor
Ali Sheikholeslami
John A. Sirevicius
Dan Sturca
Mitsutoshi Sugawar
Thomas A. Teel
David P. Tester
Frank Thiel
Antonio J. Torralba
Tsuneo Tokumitsu
Joseph Varrientos
Jean-Pierre A. Voortman
Katsuyoshi Washio



The Triumph of MOS Technology: A Book Review (continued)

This model was not replicated among the vertically organized companies, the prime example of which was IBM. IBM's voracious appetite for electronic components provided a market that supported a major manufacturing company of its own. The Solid Logic Technology (SLT), developed by IBM for the System 360 line of computers, demonstrated that a technology that would have been unsuccessful in a competitive marketplace could become a major money-maker for the company. The success of SLT eventually became an obstacle to the introduction of the much more promising MOS integrated circuit into the company's products. Bassett tells of the infighting that went on between the Research Division that was in close touch with the promise of this new technology and the Components Division that was the internal bipolar technology developer. The Components Division repeatedly reviewed Research's push for MOS integrated circuit technology and tried to shut it down, claiming that the bipolar technology would satisfy all of the company's requirements for the foreseeable future. However, their vision did not look far enough.

It was interesting that several

senior people in the Components Division were convinced by Research's story and tried to emulate the Silicon Valley start-up model with the formation of a new company, the Cogar Corporation. Having come from the IBM environment that had a large guaranteed market that none of the Silicon Valley start-ups enjoyed, and starting with between 60 and 70 people to support, Cogar ran out of money before a positive cash flow could be achieved. By contrast, Boysel started his company with a handful of people, none of whom were paid a salary initially. In fact, as successful as Intel was destined to become, it required a \$250,000,000 investment by IBM in 1982 to keep it out of financial trouble. IBM made this investment to help stabilize a domestic supplier for their integrated circuit needs.

Of course, as in much of history, there are many examples of missed opportunities. Kahng and Attalla at Bell Labs reported the invention of the MOS device in 1960, but the work was allowed to die. Hofstein and Heiman of RCA and Wanlass and Sah of Fairchild reported on the great promise of MOS technology in the winter of 1962–1963, which stimulated Landauer of IBM Research to pro-

mote the beginning of the project in IBM's Research Laboratory in Yorktown. RCA did take the technology very seriously, but Fairchild did not, and Wanlass left to spread the message elsewhere while Sah joined the academic world. RCA started a major project with government support on CMOS using Silicon on Sapphire, but government support sometimes can be a double-edged sword, requiring delivery of results that may not be useful in the time frame of the commitment. RCA and Fairchild are no longer factors in integrated circuit technology. IBM, on the other hand, is a major player in CMOS integrated circuit technology.

Bassett's book is an exciting, fast moving, and entertaining look at the early days of the MOS device development, bringing to light the remarkable interplay of people and companies that made it a dominant electronic technology. ●



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Beyond Brainstorming: A Book Review

The Art of Innovation by Tom Kelley with Jonathan Littman, A Currency Book published by Doubleday, 2001. ISBN 0-385-49984-1

Knowing how to run does not make you a winning runner. From CEOs to engineers, people feel they know how to brainstorm, but "The Art of Innovation" by Tom Kelley with Jonathan Littman will open your eyes. It teaches lessons in creativity from IDEO, the renowned Silicon Valley design integrator. This readable and entertaining book uses anecdotes

and short case studies to illustrate its points.

Kelley advises against time-consuming polls or focus groups. Your customers might not know what they want and might even tolerate problems without acknowledging them. It's not the customers' job to be visionaries.

Kelley starts by describing the building of passionate teams made up of unique and diverse innovators. The design team starts by trying its firm's own products and competitive products. Kelley's enthusi-

asm for accomplished observers of customer behavior is infectious.

To be successful, design teams need to brainstorm regularly; Kelley prefers monthly. They aim for 100 ideas an hour. When no contracts or clients are scheduled, they practice by brainstorming on concept products, industry showpiece competitions, and their own firm's advertising case studies that may never be brought to commercial use. They always bring a prototype to a meeting and expect failure. The idea is to fail often to succeed sooner.

IDEO is an annual winner of the Industrial Design Excellence Awards, with such innovations as the original Apple mouse and the Palm Pilot V. The most important piece of equipment at this firm, whose core competency is inspiring innovation, is the Tech Box. It is made up of hundreds of indexed and annotated objects, from smart fabrics to elegant mechanisms and clever toys. Designers and engineers can rummage through the Tech Box, play with its contents, and apply ideas to their current project. The goal of the Tech Box is to inspire, break holding patterns, and prevent reinvention of the wheel. For example, how does your company's circuit-cells library need to be enhanced to make it the innovative circuits designers' toolbox?

"This well-written, well-organized and energizing guide will be a magnet for more attention."

Cahners Business Information, Inc.

Even re-engineering after a product has been successfully introduced is given a full chapter's attention. Kelley calls this Version 2. Refinement for Version 2 involves asking what you don't need. Yet he recognizes that cool accessories can capture a customer's choice. Good design, we all know, is not by committee. To brainstorm Version 2 with a team of innovators requires focused goal setting.

Every chapter serves up useful

ideas: write the advertising trailer first to understand the features of the next product; leverage ideas off of metaphors; study advanced robotics, bicycling, sailing gear, and the early adopters of cutting-edge technologies. "Tear open and use," the goal for simplicity in ubiquitously-used, well-designed consumer products, applies to this book. Right up to the end, Kelley introduces compelling new habits with memorable examples from iconic designs. ●



Anne O'Neill
SSCS Executive Director
a.oneill@ieee.org

Introducing Our New Chapters

SSCS would like to extend a warm welcome to three new chapters that have been formed this year. The Denver Chapter is chaired by Randy K. Rannow, the Hong Kong joint EDS Chapter is chaired by Dr. Hei Wong, and our new joint EDS Student Branch Chapter in Turkey is chaired by Basak Yuksel. Their plans for the year 2003 include:

Denver—The Denver Chapter has more than 220 members, with a heavy concentration in northern Colorado. The membership includes technical leaders in the area of circuits and VLSI design from various firms including LSI Logic, Agilent, Hewlett Packard, ST Microelectronics, and Intel. This new chapter plans to host meetings and events to foster both learning and the sharing of technical innovation. It also anticipates working with the local community to increase awareness of the benefits that science and engineering offer.

Hong Kong—The Hong Kong Chapter is organizing a new Conference on Electron Devices and Solid-

State Circuits in July 2003. A number of Distinguished Lecturers, eminent scholars, and researchers will attend the Conference. This conference marks the 10th anniversary of the Chapter, which originally focused on electron devices and now has expanded to include solid-state circuits. During the year the chapter will hold two seminars and one workshop. A lunch is planned to recruit student members. "Students are our future volunteers and they will be the major growing sector of their local members," concludes Dr. Wong.

Turkey—The new Turkey Student Chapter is planning seminars on compound semiconductors, MEMS, and VLSI research at Middle East Technical University (METU). METU was awarded Best IEEE Student Branch worldwide in 1999. Student membership from Turkey is up 24% thanks to the work of an active IEEE committee in that country. The August issue of The Institute reported that Yakup Bayram, Ali Aydogan, and eight students from METU and Bilkent University, both in Ankara,

formed the committee to establish sixteen new IEEE Student Branches throughout the country.

Bayram is a graduate research associate at Ohio State University and is the IEEE Columbus Section Student Activities Chair. For their work in encouraging new student branches in Turkey, Bayram and Aydogan received the 2001 IEEE Regional Activities Board Achievement Award.

The semiconductor industry in Turkey is newly developing both in the universities and industry. Most of these institutions are centered in Ankara and usually seek new graduate engineers from Middle East Technical University. There is a fine opportunity for growth in student participation in the semiconductor industry and the formation of the new SSCS Student Chapter can help make that happen. Cengiz Besikci is the Student Branch Advisor at the University.

We want to commend the Chapter Chairs, officers, and members for their hard work and dedication in forming these new chapters. ●

Banner Year for SSCS Chapters



Over the last year the Novosibirsk Student Chapter has sent participants to a national conference for young semiconductor physicists in St. Petersburg, to a Siberian Electron Devices and Materials student conference in Tomsk, and to an IEEE student branch congress in Cairo, Egypt. Each July they assist in organizing the Siberian Russian Workshop on Electron Devices and Materials. In 2003 they will focus on a Solid-State Circuits session of the workshop. In 2002 they hosted the 2nd IEEE Siberian Russian Chapter Chairs meeting and two technical presentations on microsystem technology and problems in electronics instrument engineering. Pictured here at a planning meeting are (front row, left to right) Daria A. Langueva, Victoria Malutina-Bronskaya, and Svetlana V. Zaozemova; (middle row, left to right) Vladimir A. Kolchuzhin, Oleg V. Lobach, and Alexey V. Shaporin; (back row, left to right) Dmitry S. Vilmitsky, Alexander V. Nazin, and Nicolay M. Shmakov.

The Nizhny Novgorod joint Chapter, pictured at the Technological Center of Nizhny Novgorod State University when Vijay Arora delivered his EDS Distinguished Lecture, "Quantum engineering of nanoelectronic devices" (left to right): E. Shor, "Salut-27," an academic and industry joint enterprise; A. Yaschinin, Instructor of Measuring Systems, SSC-S; Professor V. Arora, visiting EDS Distinguished Lecturer; Professor Yu. Belov, the Chapter Chair; Professor V. Kiselev, Instructor of Measuring Systems, SSC-S; Professor V. Skupov, Instructor of Measuring Systems, SSC-S; Dr. V. Vdovin, Applied Physics Inst., MTT-S; Dr. S Sukhotin, Instructor of Radio Communication, CPMT-S; Dr. V.Tensin, Instructor of Measuring Systems, MTT-S. During March 2003 the Nizhny Novgorod Chapter is planning both an International Workshop on "Scanning probe microscopy" and an All-Russian Workshop on "Nanophotonics."



News from IEEE

Edison Exhibit

The IEEE History Center has added the exhibit "Thomas Edison: A Lifetime of Invention" to the IEEE Virtual Museum Web site. The exhibit explores the highlights and missteps of Edison's career, re-examines his most famous innovations, and sheds light on some lesser-known achievements. Interactive techniques demonstrate how Edison's technologies actually work. For more information, visit www.ieee-virtual-museum.org/.

Receive Discount on MIT Advanced Study Program Courses

The Massachusetts Institute of Technology Advanced Study Program (MIT ASP) has become an IEEE Education Partner. IEEE members can now continue their lifelong learning with graduate-level, credit courses provided by MIT at a 10% discount. Taught by MIT faculty, the online delivery takes advantage of the latest technologies for working engineers to keep pace with develop-

ments in their fields or to enlarge their knowledge base. Admission is based on the applicant's academic and professional background.

Applications, course prerequisites, and systems requirements are detailed at the MIT-supplied Web site for IEEE members. You must use your IEEE member number to receive the 10% discount. IEEE offers discounts for a host of University and Corporate Education Partners. Enter through the IEEE Educational Partners (www.ieee.org/EduPartners) to investigate the offerings of these partners.

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- National Technological University
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- Pace University

An Event of Topical and Regional Interest to our Members

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2002 DVD Archive includes All of the VLSI Circuits Symposium Digests

The 2002 edition of the ever popular DVD, the *IEEE Solid-State Circuits Digital Archive 2002*, will be available in February 2003. The 2002 DVD provides more content than the 2000 edition. It adds the most recent two years of *JSSC* articles and *ISSCC* papers, and includes the *Digest of the Symposium on VLSI Circuits*, previously unavailable in a single compilation. The 2002 DVD contains all the articles of the premier technical journal and two premier conferences in solid-state circuits from their inception.

- *Journal of Solid-State Circuits* 1966 through 2002
- *ISSCC* 1955 through 2002 including the slide supplements from 1990
- *Digest of the Symposium on VLSI Circuits* 1988 through 2002

TITLE: *IEEE Solid-State Circuits Digital Archive 2002*

PRODUCT NUMBER: JD3755B

IEEE MEMBER PRICE: \$120

List Price: \$800

TO ORDER: +1 800 678 IEEE (phone within U.S. and Canada)
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sscs.org/archive (order online)

Like the original DVD Archive issued in 2000, the articles in pdf can be located through a user-friendly browser portal by author, issue, or a subject index. Acrobat Reader provides Boolean and full-text searching. Tables of contents look the same as the familiar printed versions. This DVD is an important resource for all the presentations in the *ISSCC* Slide Supple-

ments that began in 1990.

The DVD will be released at the 2003 *ISSCC* and will be included with the registration fee. All of this information also is accessible online through *IEEE Xplore™* (see table) and members should compare the price versus utility for their choice. Many university and company libraries also have purchased online access to this information. ●

Availability Solid-State Circuits Articles in pdf				
	IEEE Solid-State Circuits Digital Archive 2002 (DVD)	SSCS Conference Digital Library (online through <i>IEEE Xplore™</i>)	IEEE Member Digital Library (online through <i>IEEE Xplore™</i>)	IEEE Article Purchase Online
Includes	<ul style="list-style-type: none"> • <i>Journal of Solid-State Circuits</i> from 1966 through 2002 • International Solid-State Circuits Conference from 1955 through 2002 • Symposium on VLSI Circuits from 1988 through 2002 	<ul style="list-style-type: none"> • International Solid-State Circuits Conference from 1955 to the present • Custom Integrated Circuits Conference from 1988 to the present • Symposium on VLSI Circuits from 1988 to the present 	<ul style="list-style-type: none"> • 25 articles per month • Transactions, conferences, and magazines Excludes: IEE articles and IEEE standards 	<ul style="list-style-type: none"> • Transactions, conferences, and magazines Excludes: IEE articles and IEEE standards
Member fee	\$120 for IEEE members	\$75/yr for SSCS members only	\$35/month billed monthly for 12 months	\$13 per pdf file
To purchase	sscs.org/archive	www.ieee.org/addservices	www.ieee.org/addservices	www.ieee.org/ieeexplore

The IEEE Solid-State Circuits Award

On Whose Shoulders Do You Stand?

How can so many engineers design million-transistor circuits with confidence and get reliable products to market on time? What technical advances and what algorithms are almost intuitive in our design and software processes? How do we know where to start, where it is still too risky to invest time, or what is too risky to tweak? If you can remember a decade or more ago when you dreamed about the work your team accomplishes today, you can remember the seminal ideas that have allowed circuits to evolve a hundredfold. You could be a nominator for the IEEE Solid-State Circuits Technical Field Award, the Institute's highest honor for outstanding contributions in our field.

Since its establishment in the 1980s this award has reflected the progress of the technology. The history of the field is the textbook for tomorrow's engineers. How is it that engineers can design faster, smaller, and denser circuitry every year? Look back, look around. Most of the ideas and authors are probably on the *Solid-State Circuits Digital Archive* DVD.

The Solid-State Circuits Technical Field Award consists of a bronze medal, a certificate, and a \$10,000 cash prize, and is presented at ISSCC. It honors an individual, or team of up to three, for outstanding contributions in the field of solid-state circuits, as exemplified by enhancement to technology, benefit to society, and professional leadership. The nomination form is available to download online:

www.ieee.org/about/awards/noms/solidnom.htm.

Guidelines, also available online, emphasize the importance of the nominee's accomplishments, the quality of the nomination itself, and the quality of the supporting endorsement letters. The true merits of a candidate need to be conveyed through the nomination and endorsement paperwork. The deadline for receipt of nomination materials (including the nomination form and the supporting letters) is 31 January 2003.

For further information, to coordinate your efforts with others, or to determine if a nomination is already in progress, please contact Richard C. Jaeger, the Chair of the SSCS Awards Committee, at:

jaeger@eng.auburn.edu. ●

Past Solid-State Circuits Award Recipients

2003

Daniel Dobberpuhl

Broadcom

"For pioneering design of high-speed and low-power microprocessors"

2002

Chenming Hu

Taiwan Semiconductor Manufacturing Company

Ping K. Ko

Authosis, Inc.

Quarry Bay, Hong Kong

"For BSIM3 modeling and development work"

2001

No award

2000

Robert H. Krambeck

Tandem Computers (Retired)

Hung-Fai (Stephen) Law

Alaris, Inc.

"For pioneering the introduction and implementation of domino CMOS logic"

1999

Kensall D. Wise

University of Michigan

"For pioneering contributions to the development of solid-state sensors, circuits, and integrated sensing systems"

1998

Nicky Chau-Chun Lu

Etron Technology Inc.

"For pioneering contributions to high-speed dynamic memory design and cell technology"

1997

Robert W. Brodersen

University of California, Berkeley, CA

"For contributions to the design of integrated circuits for signal processing systems"

1996

Rudy J. Van De Plassche

Philips Research Labs

"For pioneering contributions to the design of integrated circuits for data conversion"

1995

Lewis M. Terman

IBM - T. J. Watson Research Center

"For leadership in the field of MOS devices and circuits for semiconductor memories"

1994

Paul R. Gray

University of California, Berkeley, CA

"For contributions to analog integrated circuit design, especially for MOS switched capacitor circuits"

1993

Kiyoo Itoh

Hitachi, Ltd.

"For technical contributions to folded data-line circuits and the development of high-density dynamic RAMs"

1992

Barrie Gilbert

Analog Devices

"For contributions to non-linear analog signal-processing circuits"

1991

Frank Wanlass

Standard Micro Systems

"For the invention of Complementary MOS (CMOS) Logic Circuitry"

1990

Toshiaki Masuhara

Hitachi, Ltd.

"For pioneering contributions to NMOS depletion-load circuits and the development of high-speed CMOS memories."

1989

James D. Meindl

Georgia Institute of Technology

"For contributions to solid-state circuits and solid-state circuit technology"

Managing Your SSCS Membership

More choices put you in charge. In 2003 your membership can be Web based. More than half of IEEE member renewals now occur online and their renewal reminders went out in October by email, not regular post. SSCS membership now includes only the online access to the *JSSC*, and the Society's first choice for newsletter delivery is a linked email table of contents as well. (See "Your Last Copy" page 16.)

Are you worried that without the red *Journal* cover in your mailbox each month, reminding you to stay on top of circuit innovation, that you'll lose your cutting edge?

	<i>JSSC</i>	<i>Newsletter</i>
Web-based	Included with \$14 dues. www.ieee.org/jssc	Always available online. sscs.org/sscn
Email alert to table of contents	At YOUR initiative. www.ieee.org/alerts	Included if IEEE has your correct email address. You can opt out. sscs.org/e-news
Print	\$16 subscription	Included if IEEE has no email for you or at your choice.

You can see the *Journal's* table of contents as soon as it's posted by subscribing to our monthly email

alert. Go to www.ieee.org/alerts to sign-up. ●

SSCS EVENTS CALENDAR (continued from back cover)

Also posted on www.sscs.org/meetings

Technically Co-sponsored Meetings

2003 International Symposium on VLSI Technology, Systems, and Applications VLSI-TSA
vlsitsa.itri.org.tw/program/general.asp
23–25 April 2003
Hsinchu, Taiwan
Submission deadline: passed

2003 Radio Frequency Integrated Circuits Symposium
www.rfic2003.org/
8–13 June 2003
Philadelphia, PA, USA
Submission deadline: passed

2003 ACM/IEEE Design Automation Conference
www.dac.com/
2–6 June 2003
Anaheim Convention Center, Anaheim, CA, USA
Submission deadline: passed

2003 Symposium on VLSI Technology
www.vlisymposium.org
10–12 June 2003
Rihga Royal Hotel, Kyoto, Japan
Deadline for abstracts: 7 January 2003

2003 International Symposium on Low-Power Electronics and Design
poppy.snu.ac.kr/~islped
25–27 August 2003
Seoul, South Korea
Abstract deadline: 2 February 2003

2003 European Solid-State Circuits Conference
www.esscirc.org/
16–18 September 2003
Lisbon, Portugal
Paper deadline: 5 April 2003

2003 Bipolar/BiCMOS Circuits and Technology Meeting
www.ieee-bctm.org/
28–30 September 2003
Toulouse, France
Abstract deadline: 7 March 2003

2003 GaAsIC Symposium
www.gaasic.org/
21–23 October 2003
Monterey, CA, USA
Paper deadline: 7 March 2003

Your Last Copy

This could be your last print copy of the SSCS newsletter. Beginning January 2003, members will receive an email of the table of contents of each newsletter, linked to the full text posted online. All SSCS members with valid email addresses in the IEEE member database are being sent this issue's table of contents. Starting with the April issue, print copies will be mailed only to those members who have no email or who have indicated their preference to continue receiving the print copy. Web forms have been set up to capture that choice. See the table "Managing Your Membership" for URLs.

According to last winter's membership satisfaction survey, 63% of SSCS members would like electronic notice of Society news. Some members still appreciate the layout of the print version that arrives in their mailbox without prompting and can be read untethered. SSCS is making either or both options available. The AdCom anticipates a savings of \$10,000 to \$20,000 in printing and mailing costs annually, depending on how many members prefer electronic distribution of Society news.

If you did not receive an email notice of the January *SSCS Newsletter* table of contents and would like to in April, be sure that IEEE has your correct email address. Send it to address-change@ieee.org.

SSCS EVENTS CALENDAR

Also posted on www.sscs.org/meetings

2003 ISSCC International Solid-State Circuits Conference

www.isscc.org

9–13 February 2003

San Francisco Marriott Hotel, San Francisco, CA, USA

Paper deadline: passed

Contact: Courtesy Associates, ISSCC@courtesyassoc.com

2003 Symposium on VLSI Circuits

www.vlssymposium.org

12–15 June 2003

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Deadline for abstracts: 7 January 2003

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2003 CICC Custom Integrated Circuits Conference

www.his.com/~cicc

21–24 September 2003

DoubleTree Hotel, San Jose, CA, USA

Contact: Melissa Widerkehr, cicc@his.com

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