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SOLID-STATE CIRCUITS

IEEE Solid-State Circuits Society Quarterly Newsletter



CICC Celebrates 26 Years of Innovation, Education, and Communication

The 2004 Custom Integrated Circuits Conference (CICC04), a premier conference for information on leading-edge analog and digital circuits, celebrates its 26th year, 3–6 October, in Orlando, Florida. CICC is dedicated to IC development, showcasing original first-published technical work and innovative circuit techniques tackling practical problems.

CICC has evolved with the industry to cover a broad spectrum of

technical topics and offers attendees a total educational experience, including paper presentations, exhibits, panels, tutorials, and interesting networking events.

This year the program consists of in-depth educational sessions, advanced technical sessions (including sessions on emerging technology), panel discussions, technical/commercial exhibits, exhibitor preview sessions, and networking opportunities.

- Continuous-Time $\Sigma\Delta$ ADCs—K. Philips
- Device Mismatch for Data Converter Design—P. Drennan
- Digitally Assisted Analog-to-Digital Converters—B. Boser

High-Performance and Low-Power Microprocessor Design Strategies

- Low-Power Design Challenges and Techniques—L. Clark
- High-Speed Arithmetic and Logic Technologies for Beyond 65 nm: Challenges and Opportunities—R. Krishnamurthy
- Issues for Memories Embedded in Processors—B. Prince
- SOI Technology Design Challenges and Solutions—R. Joshi

Educational Sessions—Sunday, 3 October

The conference starts with three full-day educational sessions on Sunday, 3 October. These sessions are taught by practicing experts working at the leading edge of their fields. The topics for these sessions are:

Advanced RF: CAD Topics

- RF Integrated Circuit Design Using Parasitic-Award Optimization Methods—D. Alstot
- Modeling and Simulation Issues in Phased-Locked Systems—B. Razavi
- Advanced Analysis Methods and Simulation Tools for Noise in VCOs and PLLs—J. Roychowdhury and A. Mehrotra
- RF System Design Tools and Technology Tradeoffs—P. Wambacq

Advanced Data Converter Design Techniques

- Introduction to $\Sigma\Delta$ Data Converters—M. Miller

Technical Program, Monday, 4 October—Wednesday, 6 October

Keynote Presentation

CICC is very proud to announce the keynote speaker for 2004 is Dr. Chenming Hu, Chief Technology Officer, TSMC. His presentation is titled “CMOS for one more century?” It is not too early to search for the post-CMOS technology. Ideally, the new technology would have an architecture that requires only near neighbor communication to eliminate the delay/noise of global interconnects, greatly reduced power consumption, low cost, and the ability to perform functions now provided by CMOS. If a more competitive technology than CMOS cannot be found, CMOS may have to serve the

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world's need for intelligent devices and communication through this century. Can CMOS answer the call to duty?

Dr. Hu is on leave from the University of California, Berkeley, where he is TSMC Distinguished Professor of electrical engineering and computer science. His research area is micro-electronic devices and technologies. He has authored or coauthored five books and over 750 research papers. He leads the development of the BSIM transistor model for CMOS circuit simulation. BSIM is the industry standard for IC simulation and is used in the design of most ICs worldwide. He is a co-developer of FinFET. In 1997 Dr. Hu received the IEEE Jack A. Morton Award for contributions to MOSFET reliability physics. In 1999 he received the DARPA Most Significant Technological Accomplishment

Award for FinFET. In 2002 he received the IEEE Solid-State Circuits Field Award "For BSIM3 modeling and development work."

Technical Session Topics

As always, the technical sessions are highlighted by invited and tutorial papers presented by leading experts from both industry and academia. This year we have many excellent papers, especially in the areas related to emerging technologies:

Advanced MOSFET Modeling—RF and mixed-signal design continue to depend critically on the availability of accurate and realistic device models. This session contains four papers on new developments in MOSFET models, including a non-quasi static MOSFET model, models for accurate distortion analysis, the

next generation BSIM model, and a model that reflects random-dopant variations in MOSFETs.

High-Speed Serial Links—This session highlights the latest advances in high-speed serial links, employing signal processing techniques and novel circuit topologies to improve transceiver performance for low-bandwidth and low-power environments.

Analog Filters—Advanced analog filters are presented and techniques for accurate tuning and low distortion are discussed. Filters for dual-mode transceivers and a high bandwidth of 500 MHz also are demonstrated.

Challenges and Tradeoffs of SOC vs SIP—This session explores SIP and SOC trade-offs for integration of memories, analog and RF. Also presented are an MRAM replacing flash in an SIP and a fully integrated GPS IC.

Specialized Custom Circuits—This session focuses on custom circuits that cover the spectrum of frequency hopping, power management, sizing for subthreshold operation, inductive cross-talk management, and voltage doubling.

Simulation and Modeling for RF and Mixed-Signal Designs—This session presents automated macro modeling techniques for linear and nonlinear circuits followed by advanced simulation techniques for RF designs.

High-Performance Clocking and Digital Synthesis—This session showcases low-jitter, wide-range, and DLL and PLL circuits for high-speed serial links. Also included are efficient direct digital frequency synthesizer architectures.

Precision-Level Output Devices—This session presents new techniques to reduce errors in digital-to-analog converters. The second part of the session looks at data converters that produce I-bit output streams for output drivers.

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For detailed contact information, see the Society Web page: www.sscs.org

For questions regarding Society business, contact the SSCS Executive Office. Contributions for the July 2004 issue of the newsletter **must be received by 1 August 2004** at the SSCS Executive Office.

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Design for Testability—Enhancing the testability of a circuit design allows for improved product quality at reduced cost. This session includes novel techniques for high-speed I/Os, A/O converters, and $\Sigma\Delta$ modulators.

CMOS Scaling and Alternatives—This session covers the conventional bulk CMOS scaling roadmap for both digital and RF applications, as well as alternative CMOS structures that could overcome roadblocks to scaling.

ESD Protection—This session addresses a key element of IC reliability through presentation of silicon-proven approaches to 3D ESD circuit simulation, analysis of power networks, and design window expansion.

Integrated Oscillators and Tuning Elements—The session begins with a discussion of MEMS for wireless applications. Two VCOs that achieve a wide tuning range by means of switched capacitor techniques are presented next. Finally, techniques for temperature desensitization and for inductor size optimization are proposed.

Custom Circuits for Interfaces and Imaging—Circuit ideas for read channel, audio, and image-sensing applications are discussed with emphasis on high-speed, low-power, or low-noise considerations.

SOC Solutions for Nanometer Design—As SOC process technology scales, many problems ensue. This session starts with DFM, then discusses power management and different design techniques to pro-

vide insight into these problems and their solutions.

Advanced Memory Issues—This session presents solutions to issues affecting advanced memories, including power reduction, speed improvement, process defect tolerance, and soft-error correction.

RF Noise Modeling and Analysis—This session offers advanced research results on flicker and HF noise modeling and characterization, and on coupling analysis for RF components, circuits, and substrate.

Single-Chip Radio Solutions for Wireless Communication—A fully integrated 1-V Bluetooth transceiver, a ultra-low-power 900-MHz transceiver, single-chip implementations for wireless LAN applications, and an IF-digitizing IC for EDGE/GSM base solutions are presented.

Programmable Architectures — Technology advances for each major type of programmable device applicable to a wide range of digital system designs are addressed. Presentations include via-programmable, metal programmable, synthesizable cores, CPLDs, and the complex issue of I/O design for high-performance FPGAs.

Memory Trends—This session presents trends in memories, including challenges in embedded and emerging memory, future embedded DRAM using single-electron concepts, advanced ternary CAM, and anti-fuse.

Interconnect and Noise Modeling—This session covers inductance and

capacitance extraction methods, interconnect modeling, noise coupling, and dynamic power-integrity analysis.

Over-Sampled Analog-to-Digital Converters—This session is comprised of papers that describe low-power and multi-bit techniques for the development of over-sampled analog-to-digital converters for low-pass applications.

Wireless Transmitters—The session begins with an invited talk presenting SOI technology for RF applications. Subsequent papers present new methods for transmitter design, including polar and digital modulation techniques.

Signal and Data Processors—This session presents recent advances in integrated circuits employing programmable and reconfigurable architectures for low-power, high-performance communications and multimedia signal-processing applications.

Broadband Circuits and Frequency Synthesis—Techniques for broadband circuit design are proposed. Applications include an LNA for ultra-wideband, a DC-10-GHz attenuator, a Ku-band tuner for satellite applications and a 21–27-GHz power combiner. The session also explores two fast locking frequency synthesizers and a technique for improved frequency ratio measurements.

Analog Techniques—Analog circuits rely on low-voltage references, on good component matching, and often on trimming circuits. Furthermore, high-speed operation frequently relies on advanced processes and innovative circuits.

Introduction to Silicon Debug and SOC Test—This invited session includes tutorial-style presentations on the challenges of silicon debug and one company's approach to implementing a proposed IEEE standard on modular SOC test.

Panel Discussions – Tuesday October 5th

Three spirited panel discussions will feature experts sure to offer strong opinions on the following topics:

MEMS and Nanotechnology—Hot or Hype?

Are ASICs Dying Because of FPGAs and the Price of Software?

SOC vs SIP: Are We Putting Too Much on One Chip?

CICC Celebrates 26 Years *Continued from page 1*

Emerging Technologies in SIP and SOC—This session presents the latest innovations in technologies integrating SIP and SOC, including MEMS, antennas, thin-film inductors, and sensors.

Low-Power Issues for FPGAs—Power issues have emerged as a key concern for the design of modern FPGAs, especially at 90 nm and beyond. This session discusses these concerns and suggests some solutions.

Exhibits— 4–5 October

Monday afternoon the exhibitor preview sessions kick off the opening of the exhibit hall. Here many of our exhibitors will present overviews of new products and services.

As always, our exhibits will include displays and demonstrations by semiconductor manufacturers, software tool suppliers, design service houses, and leading electronics industry publications providing the latest technical information on new integrated circuit design products.

The exhibit hall will be the site for Monday's exhibitors' reception and Tuesday evening's happy hour, providing opportunities for attendees to network with their colleagues and the exhibitors.

Luncheon Presentation— 5 October

The luncheon guest speaker, Dr. Frederic Zenhausern, is the director of the Applied Nano-Bioscience Center (ANBC) at Arizona State University. His presentation, "Impact of

nanoscale science on life sciences and medicine," will address the area of technology and medicine. Today, when a patient is diagnosed with cancer, often large areas of tissue or even entire organs have already become affected. But these diseases started small at some stage, within a single cell at the level of molecules and atoms. The aim of the "Nanoscale life science" projects at the Center for Applied Nanobioscience is to create tools that will enable the first pathological changes to be studied and diagnosed. In nature everything starts from a single cell, which contains the genome, and that information is used to build an entire organism. The center is developing integrated and miniaturized systems for robust and rapid nucleic acid diagnostic testing.

Recent progress in designing new devices will be reported for various applications ranging from basic research to human identification. For example, prototypes will be described for pharmacogenomic diagnostics to predict patient responsiveness to cancer treatments, detect exposure to bioterror agents, and screen subjects for clinical trials. The first platform is on melanoma treatment that builds upon joint work at TGen and ANBC. Platform architectures can comprise a multifunction nanofluidic array with small spot density of < 100 to perform hybridization-based bioassay ten times faster than conventional microarrays. Integrated platforms with on-chip sample preparation also will be reported

for fully automated diagnostics.

As the fabrication of emerging nanoscale devices demands a patterning technology that is capable of sub-10-nm resolution, which is beyond the capability of any traditional lithography technologies, including electron beam lithography, ANBC will report its approaches and recent progress in developing an unconventional patterning technology of polymeric substrates. Such technology will allow fabricating devices with dimensions closer to molecular scale offering interesting ways to manipulate single molecules in a confined environment. For example, applications to DNA mapping will be illustrated. Finally, the impact of miniaturization and integration of analog circuitry and sensors on flexible substrate also will enable designing new low-cost disposable platforms for biosensing.

Caribe Royale Resort Suites, Orlando, Florida

The conference will take place at the Caribe Royale Resort Suites in Orlando, Florida. The Caribe Royale is an all-suites hotel. Every room has a bedroom and a living/dining room. Parking at the hotel is free. The hotel is only 1.5 miles from the Walt Disney World Resorts®. The hotel features five restaurants, an exercise room, an outdoor swimming pool with water slide, and a hot tub. The hotel Web site is www.cariberoyale.com.

For additional information see www.ieee-cicc.org ●

The CD of the JSSC 2002-2003

was mailed to subscribers 15 June 2004.

Non-subscribers may order a copy online.
shop.ieee.org/store/product.asp?prodno=JC18104

Member price \$30



Nagaraj Named New Editor-in-Chief for *JSSC*

Krishnaswamy Nagaraj was appointed the new the Editor-in-Chief for the *IEEE Journal of Solid-State Circuits* at the 15 February meeting of the Society's Administrative Committee.

Dr. Nagaraj was an associate editor of the *Journal of Solid-State Circuits* from 1998 to 2002 and was a member of the ISSCC technical program committee from 2002 to 2004. He has been with Texas Instruments since 1996. Until recently he was at the Texas Instruments Design Center in Warren, New Jersey, where he led a team engaged in the design of mixed-signal integrated circuits for hard disk drives, wireless LANs, and wireless base stations. During the same time he

also was an adjunct associate professor at the University of Pennsylvania. He is presently with the Wireless Terminal Business Unit of Texas Instruments in Dallas, Texas.

Krishnaswamy Nagaraj obtained his BE degree in electronics from Bangalore University in 1972 and his ME and PhD degrees in electrical communications engineering from the Indian Institute of Science, Bangalore, in 1974 and 1983, respectively. From 1974 to 1984, he was with the R&D laboratories at the Indian Telephone Industries, Bangalore, where he was engaged in the design of digital communication systems.



From 1985 to 1986 he was with the University of Waterloo, Canada, where he taught and researched analog integrated circuits. From 1986 to 1996 he was with Bell Laboratories in Murray Hill, New Jersey, and Allentown, Pennsylvania, where he was involved with the design of mixed-signal integrated circuits for telecommunications and data storage.

Nagaraj's term will begin with the July issue of the *JSSC*, replacing Bernhard Boser of the University of California, Davis, who has served since 2001. ●

Congratulations New Senior Members

Lutfi Albasha
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The screenshot shows the IEEE Xplore website interface. At the top, there are navigation links: IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE. Below this is the IEEE Xplore logo and a welcome message for SHASHI K. MULLER. The main content area is titled 'Full-text Search Prototype' and includes instructions for using the search feature. It lists steps: 1) Enter keywords in one or more text boxes, 2) Select the fields to search for each keyword, 3) Select search operators when using multiple keywords, 4) Limit the results by selecting Search Options, and 5) Click Search. The interface also features a 'Search Options' section with checkboxes for 'IEEE Journals', 'IEEE Journals', 'IEEE Conference proceedings', 'IEEE Conference proceedings', and 'IEEE Standards'. There are also fields for 'Select years to search' (From year: All, to: Present) and 'Organize search results by' (Sort by: Relevance, order: Descending, List: 15 Results per page).

Full-text search is now available in IEEE Xplore® Release 1.7. This new feature, released on 29 April, is a prototype that enables the search of metadata fields and the associated full-text journal/transaction content from 1996 forward. This currently represents more than 10% of the content in the database. The remaining content will be included in the full-text search function by the end of the year. For more information, visit ieeexplore.ieee.org/xpl/ReleaseNotes.jsp.

New Journal of Display Technology Will Launch in 2005



The new *IEEE Journal of Display Technology* will launch in 2005 with SSCS as a co-sponsor to the initiative begun by the Lasers and Electro-Optics Society. Five other IEEE societies will also cosponsor with two additional considering sponsorship and the Optical Society of America, also considering cosponsorship.

One of the objectives of the new *Journal* is to encourage technical societies to develop a broader interest in display technology and to begin to more effectively address the needs of members working in this technology.

The steering committee and editorial board of the new *Journal* will be formed as soon as the IEEE

Technical Activities Board provides final approval at their June meeting. The editorial board will issue a call for papers. Author submissions will be via Manuscript Central and the *Journal* will be peer-reviewed.

The plans state beginning quarterly publication in 2005 with a member rate of \$25 for online, \$27 for print, and \$38 for both. Subscriptions will be available during the 2005 renewal drive this fall. Institutions that already subscribe to all IEEE offerings through *Xplore*, will have automatic access to the new publication. The *Journal* will utilize “rapid-posting,” that is, as soon as an article is edited for publication, the staff-formatted version will be posted in *Xplore*. At the time

the *Journal* is printed, the version with page numbers and issue ID suitable for citation referencing will replace the earlier online pre-print copy.

The scope of the *Journal of Display Technology* will be the theory, design, fabrication, manufacturing, and application of information displays and aspects of display technology that emphasize the progress in device engineering, device design, materials, electronics, physics, reliability, and human-factor aspects of displays and the application of displays. Given the breadth of the topic, from basic materials, components, systems, and equipment to human factors, and the lack of depth in any one or even a few societies, this is a perfect candidate for a cosponsored publication. No single IEEE entity covers displays in any complete sense, although there are some solid, focused activities within a few IEEE societies, and related technical activities in many societies.

Display technology is driven by the rapid changes in the information technology industry and has grown to be a \$100-billion industry. Displays are key component technologies for many electronic systems, and the primary means for visual communication. Although the market for CRT monitors is declining, all other segments forecast growth: LCD monitors, PDP systems, CRT television, rear projection, and front projection. According to market projections at Stanford Resources, growth in the display industry is expected to accelerate over the next ten years, with cumulative growth rates exceeding 10–18% per year.

The five other cosponsoring IEEE societies are: Electron Devices, Components Packaging and Manufacturing Technology, Broadcast Technology, Instrumentation and Measurement, and Industry Applications. ●

Fourth IEEE Asia-Pacific ASIC Conference in Fukuoka, Japan, 4-5 August 2004



Pictured from left to right: Lee, Matsuzawa, Chen, and Usami.

The fourth IEEE Asia-Pacific Conference on Advanced System Integrated Circuits (AP-ASIC) will have 88 paper presentations, four invited talks, and one panel discussion.

Invited Talks

The first invited talk is “An ultra-small RFID chip: mu-chip,” presented by Dr. Mitsuo Usami, Hitachi, Japan. An ultra-small (0.4 mm x 0.4 mm) radio frequency identification (RFID) chip named μ -chip has been developed for use in a wide range of individual recognition applications. The chip is designed to be thin so that it can be applied to paper and to thin paper-like media, which have been used widely in retailing to create certificates that have monetary value, as well as for token-type devices. The mu-chip has been designed and fabricated using 0.18-micron standard CMOS technology. To extend widely this RFID chip into versatile applications, another type of ultra-small (0.4 mm x 0.4 mm) antenna embedded in the chip is presented.

The second talk is “Developing SOC for digital consumer electronics,” presented by Professor Akira Matsuzawa, Tokyo Institute of Technology, Japan. This talk reviews and discusses a business strategy, a technical feature, and a development management method for SOC which is developed for digital consumer electronics. The digital consumer electronics market has been growing

and a real personal multimedia era has emerged. SOC is a key technology for this field. The media processor is a powerful solution not only to realize high-speed operation with low-power consumption, but also to strike a balance between standardization and individualization. The architecture for the media processor should be optimized for the applications to increase the performance and to decrease power consumption and cost. Mixed-signal technology becomes vital for all SOCs along with increase of the integration level in multimedia technology and digital wired and wireless networking. A new simulation method and a new development system are needed to increase the design quality and to shorten the development time in mixed-signal design. A global development management method is going to be needed to address the complicated tradeoff issues for many device parameters and for global optimization from system to silicon.

The third invited talk is “SOC R&D trends for future digital life,” presented by Dr. Ki Won Lee, CTO and Executive Vice President, Samsung Electronics, Korea. This paper depicts the future R&D direction and the importance of System-On-a-Chip (SOC) based on a forecast of the device integration trend in the Digital Convergence Era. The measures that the consumer electronics industries are taking in order to solidify the competitiveness of its set products are presented.

A new technology paradigm, Digital Convergence, is emerging. We are witnessing the coming of Network Convergence, where the conventional wired and wireless broadband network is converging into an IP-based, ubiquitous network. Device Convergence, due to the demand of the next-generation, multifunctional multimedia digital appliance, is on the horizon, as part of the Digital Convergence Ecosystem. Finally, Service Convergence, with the internet as the trigger for providing information and entertainment to customers in real-time, serves as the last building block for the Digital Convergence Era. As a whole, they promise to offer value-added solutions and revolutionize our future digital lifestyle.

In a time of such paradigm shift, the following three principles are what separate global leaders from rest of the pack in the Digital Convergence Era: developing innovative products and technologies, understanding the market and being first to the market, and establishing a global collaboration network.

The importance of SOC cannot be understated in Device Convergence, where securing your own solution is becoming even more critical in developing distinct products. With the technology landscape rapidly changing, Samsung Electronics is strategically allocating its resources in SOC R&D to gain and maintain a competitive edge in the next-generation digital appliance market. The development of innovative technologies such as the Digital Natural Image engine (DNIe) chip that improves the digital TV visual experience, embedded media process modem for mobile phones, and the CMOS Image Sensor (CIS) are examples that are described in detail.

The fourth invited talk is “Hardware architecture for visual processing: present and future,” presented by Professor Liang-Gee Chen, Director, Graduate Institute of Electronics Engineering, National Taiwan University, Taiwan.

This paper explains the present

and future trends of hardware architecture design for image and video coding. Fundamental design issues are discussed with particular emphasis on efficient dedicated implementation. Hardware architectures for MPEG-4 video coding and JPEG2000 still-image coding are reviewed as examples. Special approaches exploited to improve efficiency are identified.

Panel Discussion

Koichiro Mashiko, STARC, Japan,

will lead the discussion on “Academia/industry collaboration in SOC design education: Wishes and reality.” There seems to be a general consensus that the collaboration between academia and industry is essential to survive and grow in the SOC business. This panel focuses on the educational aspects of the collaboration programs for SOC design. First, panelists from various countries/regions and technical/managerial backgrounds will introduce their programs (ongoing or

planned) to share their views and experiences. Then, through Q&A and discussions, common problems will be identified and more effective schemes to reach productive win-win relationships between academia and industry will be explored. Issues include: curriculum/courses, infrastructure, funding, manpower, foundry service, and practical training.

For more details please visit the conference Web site at www.vdec.u-tokyo.ac.jp/AP-ASIC2004/. ●

ESSCIRC 2004 Meets 21–23 September, 2004 in Leuven, Belgium

The 30th European Solid-State Circuits Conference will be in Leuven, Belgium 21–23 September 2004. The aim of the conference is to provide an annual European forum for the presentation and discussion of recent advances in solid-state circuits and technologies. It is coorganized together with ESSDERC, which deals with solid-state devices. The increasing levels of integration for SOC design made available by advances in silicon technology is stimulating, more than ever before, the need for deeper interaction among technologists, device experts, and circuit and system designers. ESSCIRC and ESSDERC will share Plenary keynote presentations bridging both communities.

The technical advances for RF are from advanced low-noise amplifiers (up to 52 GHz) to fully-integrated low-power ISM transmitter devices. Also in the A/D and D/A area, high-speed (up to 1.6GS/s), high-accuracy (up to 120 dB/ 110dB THD+N) and low-power high-accurate current steering DACs will be presented. As usual, analog circuit design is well represented at ESSCIRC with Gb/s optical-drivers and receivers, Gm-C filters, and high-performance amplifiers. Mixed-signal sensor circuits such as tactile sensors, Hall sensor circuits and high-accurate (16 bit) sensor data-acquisition circuits will be discussed. Besides analog and mixed-mode, several digital-circuit techniques for gate-leakage suppression and memory devices will be presented.

The ESSDERC/ESSCIRC 2004 Keynote Speakers:

- Technology Considerations for Automotives — H. Casier, AMIS, Belgium
- Organic Electronics for LED Applications — R. Friends, Cambridge University, United Kingdom
- Low Voltage, Low-Power Aspects of Data Converter Design — Q. Huang, ETH, Switzerland

- Low-Power Digital Circuit Design — T. Sakurai, University of Tokyo, Japan
- Integrated Circuits for the Biology to Silicon Interface — R. Thewes, Infineon, Germany
- On Ambient Intelligence, Needful Things, and Process Technology — C. van der Poel, Philips Research Leuven, Belgium



The ESSCIRC 2004 Invited Speakers are:

- The Impact of CMOS Scaling on Analog CMOS Circuit Design And Performance — M. Vertregt, Philips, The Netherlands
- UWB Systems — J. Farserotu, CSEM, Switzerland
- DSP, a Technology, a Product, a Revolution — G. Frantz, TI, USA

In addition to the conference there will be a tutorial on Integrated optical interface circuits on Monday, 20 September, and on Friday, 24 September a workshop on multimode multiband reconfigurable systems for enhanced third generation mobile phones.

The technical program chair is Professor Michiel Steyaert, KU Leuven, Belgium. The local organizing committee chair is Professor Cor Claeys, IMEC <c.claeys@ieee.org>. For details, the technical program, and registration refer to www.esscirc.org. ●

Ultra-Wideband Wireless Chip Wins Student Design Contest

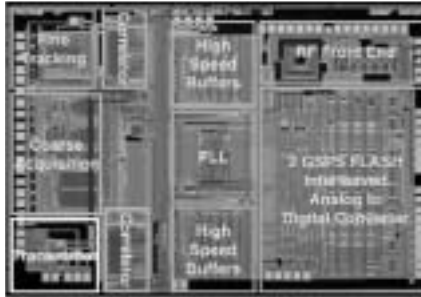
The Student Design Contest made its debut at ISSCC this year, with seven teams of students presenting poster sessions. Over the last two decades this contest has evolved into a premier international design contest for all students. Any design done by students as part of their studies is eligible. Entries cover a broad range of design styles including systems, FPGA, analog, digital, and MEMS chips. The contest has two categories. The operational category is for designs that have been fabricated and tested. The conceptual category is for designs that have been simulated extensively and include test plans, but have not yet been fabricated.

The contest was founded by Kent Smith at the University of Utah in 1981. Subsequently, it was run by Richard Brown at the University of Michigan. The Design Automation Conference (DAC) took over the competition in 2000. In 2002 ISSCC and DAC collaborated to cohost the contest. Bryan Ackland, who was instrumental in establishing the contest at ISSCC, notes "The design contest generates excitement among students about getting involved in the broader conference community."

To ensure neutrality in the contest, judges are drawn from a wide spectrum of backgrounds, including institutions sponsoring the competition, academia, and representatives from ISSCC and DAC conferences. All judges are well-respected designers in their own fields.

The design contest is steadily growing in size with a total of 59 entries this year. Details of previous competitions and winners can be found at www.dac.com/41st/student-con.html. In mid-October the 42nd DAC Web site will be available for students to submit their entries to the next contest. Detailed contest rules are available on both the DAC

and ISSCC Web sites. The submission deadline for the contest is 7 December 2004. This year judging will take place early enough for the winners to show posters at ISSCC 2005. This change enables designs



"A single-chip ultra-wideband transceiver," by Fred S. Lee, Raul Blazquez, and Puneet P. Newaskar, supervised by Professor Anantha Chandrakasan, was named the operational winner of the 2004 DAC/ISSCC Student Design Contest (out of 59 entries). This CMOS chip integrates a complete wireless transceiver system working in the 0-500-MHz ultra-wideband. The judges were impressed by the high level of integration and the demonstration of working transmission at 200 kb/s.

to be presented as soon as possible after winning in the competition. ISSCC 2005 will be a catch up year with winners from both 2004 and 2005 presenting. Winners for 2005 will be informed in early January, allowing them one month to make their preparations to present their poster at ISSCC. A limited amount of travel assistance is available to help winners attend the conference.

The design contest can be used as an incentive to students in their studies. Alan Mantooh, professor at the University of Arkansas and co-chair of the contest, comments "The contest provides value to the students in terms of completeness and design documentation—aspects that are very important in industrial settings. It helps prepare them for the next phase of their careers."

This year's operational category and overall winner is from MIT. The entry was "A single-chip ultra-wide-

band transceiver," by students Fred S. Lee, Raul Blazquez, and Puneet P. Newaskar, supervised by Professor Anantha Chandrakasan. This CMOS chip integrates a complete wireless transceiver system working in the 0-500-MHz ultra-wideband. The judges were impressed by the high level of integration and the demonstration of working transmission at 200 kb/s.

The winner in the conceptual category is from the University of Michigan, Ann Arbor. "The economical aphotic sieving machine," by Kamran Kashef and Matt Hardy tackles methods for breaking public key encryption, such as the RSA algorithm, in a much more efficient way than conventional computers.

Prize money was donated by the contests sponsors: SRC, MARCO, IEEE CASS, ACM/SIGDA. Prizes were presented in June at the San Diego DAC.

The previous years winners who presented their designs at ISSCC 2004 were:

In the operational category: "A computationally efficient ASIC implementation for the decoding of space-time block codes," by Enver Cavus, supervised by Professor Babak Daneshrad of the University of California, Los Angeles.

In the conceptual category: "A 16-bit mixed-signal microsystem with integrated CMOS-MEMS clock reference," by Robert M. Senger, Eric D. Marsman, Michael S. McCorquodale, Fadi H. Gebara, and Keith L. Kraver, supervised by Professor Richard B. Brown of the University of Michigan, Ann Arbor. ●



David Greenhill
David.Greenhill@Sun.com

2004 IEEE Fellows

Thirteen new IEEE Fellows are being honored by the IEEE for contributions close to the technical pulse of the Solid-State Circuits Society. All are SSCS members and their contributions and leadership are recognized and evaluated by our many sister societies.

An IEEE Fellow is a member of unusual distinction in the profession. This recognition is conferred only by invitation of the Board of Directors upon a person of outstanding and extraordinary qualifications and experience in IEEE designated fields, who has made important individual contributions to one or more of these fields. No more than one-tenth of one percent of the total Institute membership may be advanced to Fellow grade in any given year.

A nomination for Fellow must be accompanied by references from at least five current IEEE Fellows. A nominee must be a Senior Member of the Institute and must have been a member in any grade for at least five years prior to the year of election. Each nomination is evaluated by the relevant technical society or council and is ranked by the 26-member IEEE Fellows Committee. Multiple reviewers produce a composite viewpoint that is used in recommending to the Board of Directors suitable candidates for election to Fellow grade. For more information see www.ieee.org/fellows.

Professor Thomas Joseph Brazil
National University of Ireland,
Dublin

For contributions to circuit-level modeling of non-linear devices

Dr. Robert Howard Eklund
Texas Instruments, Plano, TX
For leadership in the development and manufacturing of sub-micron CMOS technologies

Dr. Erik H.M. Heijne
CERN, Geneva, Switzerland
For contributions to semiconductor detector systems and radiation-tolerant detector readout electronics

Chaohuan Hou
National Natural Sciences
Foundation of China, Beijing
For technical leadership in advancing VLSI system technology

Hajime Ishikawa
Fujitsu Laboratories Ltd., Kawasaki,
Japan
For technical leadership in the development of high-performance Si and GaAs devices and circuits

Dr. Masayuki Izutsu
Communications Research
Laboratory, Tokyo, Japan
For contributions to integrated optics and broadband guided-wave light modulators

Dr. Robert W. Jackson
University of Massachusetts,

Amherst
For contributions to the electromagnetic modeling of microwave integrated circuits and packaging

Hiroshi Nozawa
Kyoto University, Japan
For contributions to nonvolatile semiconductor memories

Professor Mikael Ostling
KTH, Royal Institute of Technology
Kista, Sweden
For contributions to semiconductor device technology and education

Professor Gordon Roberts
McGill University, Montreal, Canada
For contributions to the design and test of analog and mixed-signal integrated circuits, and education

Professor Mohamad A.H. Sawan
Ecole Polytechnique de Montreal,
Canada
For contributions to implantable medical devices

Dr. Stuart K. Tewksbury
Stevens Institute of Technology,
Hoboken, NJ
For contributions to telecommunications and interconnections in high-performance digital systems

David Wood
University of Wisconsin-Madison
For contributions to the design and evaluation of shared-memory multiprocessors ●

SSCS Members Vote for Division 1 Director-Elect in the Fall

SSCS members will be called upon to vote for Division 1 Director-Elect in the IEEE fall election. Starting with the 2005 term, the two-year term for all Division Directors will be preceded by a one-year term as Division Director-Elect. The purpose of the Division Director-elect term is to ensure that incoming directors learn the duties and respon-

sibilities of the position, and are up to speed on IEEE, Board, and TAB activities and considerations when they become members of the IEEE Board of Directors and TAB.

The candidates for Division 1 Director-Elect for 2005 are:

Steven J. Hillenius, former EDS President

H. Scott Hinton, current LEOS

President

Harnatha C. Reddy, former CAS President.

Whoever is elected this fall begins his term as Director-Elect in 2005, and becomes Division 1 Director for 2006–2007. As this issue goes to print, these candidates are preparing their resumes and statements for posting online.

Division 1 consists of five societies and two councils:

- Circuits and Systems Society
- Components, Packaging, and Manufacturing Technology Society
- Electron Devices Society
- Lasers and Electro-Optics Society
- Solid-State Circuits Society
- Nanotechnology Council
- Sensors Council

A Division Director serves on both TAB and the IEEE Board of Directors. The IEEE Board of Directors is the governing body of the IEEE, responsible for the operation of the Institute. It consists of ten Regional Directors, ten Division

Directors, the five major Board Vice-Presidents, Treasurer, Secretary, and the three Presidents. As part of Division 1, SSCS members vote for the Division 1 Director.

Duties of a Division Director-Elect include:

- Attending all TAB meetings, TAB caucuses, Directors' forums, and other meetings
- Attending all IEEE Board of Directors meetings
- Becoming familiar with the societies and councils in the division
- Attending at least one IEEE regional meeting per year
- Assisting the Division Director in serving the best interests of IEEE

Other positions contested in this fall's IEEE election include the IEEE President-Elect, with candidates Michael R. Lightner, Levent Onural, and James M. Tien. Running for Technical Activities Vice President-Elect for 2005 are Celia L. Desmond, James D. Isaak, and Philip T. Krein. A number of other Division Director positions, as well as Region and Standards positions, are also on the slate.

Please check the site (www.ieee.org/corporate/elections/candidates.xml) and then discuss this election and its merits with your fellow members. When the ballot arrives this fall, please cast your vote. ●

The SSCS France Chapter: Questions for Laurent Fesquet

Laurent Fesquet organizes events dynamically, taking advantage of experts' travel and hot topics. It's a success for those employed in industry but student needs are still a focus of program development.

Q: How do you plan chapter events and speakers?

There are mainly two ways that lead to a chapter activity:

1.) Most of the time, I use the traveling schedule of experts as an opportunity to invite them as speakers and organize a chapter event. For example, on June 14th a PhD defense is organized in my laboratory, TIMA. One of the jury members, Christian Piguet, is the head of the ultra-low-power circuits section of the CSEM center in Switzerland. In addition, Vojin Oklobdzija, an IEEE Distinguished Lecturer and professor at the University of California, Davis, is currently at EPFL in Switzerland too. This gave me an opportunity to organize a technical event on "Leakage, energy, and speed in digital circuits" on June 15th.

2.) Less often, we determine a hot topic with some of the active members. For instance, last year we orga-

nized a workshop on a topical subject: "System on A Chip: Design for low power." This event was held in cooperation with the French CAS chapter and ATMEL, a microelectronics company. As ATMEL had suggested this topic, we decided to organize the meeting in Rousset. For this event we invited three IEEE Distinguished Lecturers: Professor Sakurai and Professor Vladimirescu from the CAS society and Dr. Itoh from the SSCS.

Who are some of the people (not the speakers) who help you organize events for the France SSCS chapter? What do they do?

I usually find an active member interested in the topic to help me organize the event. Moreover, we have developed cooperative relationships with the CAS and the CPMT chapters to organize meetings on integrated systems. So it is possible to cover many topics, from packaging to system design.

What type of administrative meetings does your leadership hold?

Most of the time administrative meetings are not formal and are not held during a national conference. To save time, we use conference calls.



Laurent Fesquet is currently in charge of the French IEEE-SSCS Chapter. He received his engineering degree in physics from the Ecole Nationale Supérieure de Physique de Strasbourg in 1993 and his MA in applied physics from the Ecole Normale Supérieure de Cachan in 1994. He received his PhD in electrical engineering in 1997 from the University of Toulouse. Since 1999, he has been an associate professor at INPG and is working on asynchronous microelectronic systems in the TIMA laboratory.

How many people is a good number to organize and run a chapter? and why?

From my point of view, four or five people are needed to manage a chapter. A few active people are better than many inactive people.

What do you find satisfying about running the chapter?

I enjoy meeting a lot of people in the SSCS domain.

How do chapter events serve industry needs?

Most events serve industry because some of the activities are proposed

by industry members and the technical events attract primarily those employed in industry—thanks to the quality of the speakers and the choice of hot topics.

How do chapter events serve student needs?

This is difficult! Except for PhD students, it is difficult to serve student needs. Indeed, it is almost impossible to organize events with the masters and engineering students. The French educational system in science and the French student culture for the masters and engineering students makes it difficult to organize events for them.

What kind of volunteer roles are you looking to fill?

I am currently looking for volunteers to help organize student activities—unsuccessfully so far!

What else would you like your chapter to do if you had the time and the budget?

If I had enough time, I probably would edit a French journal of solid-state circuits, including chapter information and technical papers. This would help maintain contact with the members and attract more students in the domain. ●

Chapters Make SSCS Vital Around the World

SSCS chapters provide great programs for local members. Here are a few reports from some of our 48 chapters around the world. Also in these reports are ideas for members who would like to volunteer to help. France might start a local technical publication and expand services for students, while Santa Clara Valley needs a few volunteers to help run a course on RFIC design.

Atlanta



The revitalized Atlanta Chapter met 22 March and 22 April. Officers are shown on 22 March with Alan Hastings who spoke on “Safe operating area protection by power limiting.” Left to right: Patrick O’Farrell (Secretary), Gabriel Rincon-Mora (Vice-Chair), Alan Hastings (speaker), Phil Allen (Chair), and Bruce Schmukler (Treasurer).

Kansai

The Kansai chapter held a technical seminar on 29 March in Kyoto, focusing on the management of technology development as well as business issues in cutting-edge IC design companies. Two IEEE Fellows spoke, rewarding an audience that came from many regions of Japan with a stimulating presentation.

Dr. Osamu Tomisawa, professor of entrepreneur

engineering at Kochi University of Technology, lectured on both fundamental and up-to-date points of technology management, covering technology strategy and marketing in a high-tech company. He also presented case studies on corporate ventures, in particular in the United States.

Dr. Nicky Lu, President of Etron Technology Incorporated, provided an in-depth talk on “Emerging technology and business solutions for system chips,” extending his Plenary Session talk at ISSCC 2004. Heterogeneous integration of various functions into a single-system chip, as a new horizon of IC technology development, was discussed with the audience. The marketing potential of such single-system chips was examined. Discussion focused on single-system chips that use technologies already available as well as those technologies yet to be developed. Strategic borderless partnerships among versatile companies ranging from vertical integration to horizontal segmentation were also examined. The nonstop discussions between the audience and the lecturers continued until the end, characterizing the success of the seminar.



Kansai Chapter meeting sponsored two IEEE Fellow presentations. Left to right: Junji Ishikawa (Treasurer), speakers Nicky Lu and Osamu Tomisawa, Masao Nakaya (Chapter Chair), and Makoto Nagata (Secretary).

Denver

Following the inaugural year anniversary in September 2003, the SSCS Denver Chapter continued hosting monthly technical seminars covering a broad range of topics on circuits and devices. In October 2003 Don Bartlett (Greyrock Technology), a local entrepreneur, shared his insights and perspectives on developing a small engineering business. The following month, Dr. Jeremy Theil (Agilent Technologies) gave a technology overview of monolithic instruments on silicon and touched on growing trends such as embedded image sensors.

We were extremely pleased that our two most recent seminars drew our largest-ever crowds of 50–60 people. In March 2004 we were honored to host Professor Eric Vittoz (CSEM, Switzerland), who had recently received the prestigious IEEE Solid-State Circuits Technical Field Award at ISSCC 2004 in San Francisco. He delivered a much-anticipated Distinguished Lecture on the fundamental properties of MOS transistors and applications for low-power circuits. Participants were thrilled to finally meet the pioneer who had developed the subthreshold MOS techniques that are now commonplace in the design community. The following month, Minh Quach of Agilent Technologies delivered a very informative lecture on signal integrity considerations and analysis that included a practical tutorial on high-speed test and measurement techniques.

During the past months, the officers have been involved in a couple of community service events. During Engineering Week in February, Chapter Chair Dr. Don McGrath spoke at three local high schools to encourage students to continue their education in science and engineering. In early April the entire officer team served as science fair judges at a local bilingual (English/Spanish) elementary school. Officers were impressed with the creativity and scientific rigor demonstrated by kids as young as third graders. For example, one student learned that chemiluminescence in glow sticks was an activated process. Another student inadvertently embarked on a blackbody radiation experiment to explain why her white cat enjoyed lounging in the afternoon sun longer than her black cat.

We look forward to growing participation in upcoming seminars. We are encouraged that the technical seminars, as well as a social event hosted at a local clubhouse, are providing networking opportunities for the local members. Some members have re-established employment based on leads shared during these meetings.

Please visit our Web site at <http://ewh.ieee.org/r5/denver/sscs/> for more information (including past presentation slides) about our chapter events. ●

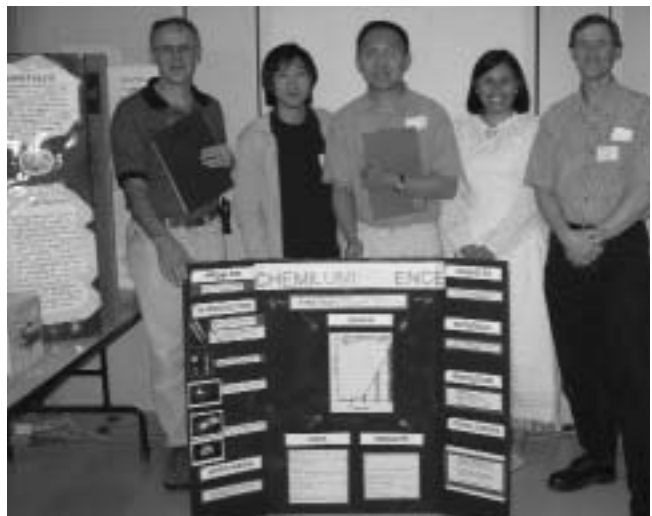
Alvin Loke

Denver Chapter Vice Chair

alvin.loke@ieee.org



The Denver Chapter hosted a seminar in March (left to right): Don McGrath (Chapter Chair), Professor Eric Vittoz (Distinguished Lecturer), Bob Barnes (Treasurer), Tin Tin Wee (Secretary/Web master), and Alvin Loke (Vice Chair).



The Denver SSCS Chapter officers judged a local elementary school science fair in April 2004 (left to right): Bob Barnes (Treasurer), Tin Tin Wee (Secretary/Web master), Alvin Loke (Vice Chair), Isabel Chavez-McBeth (teacher at Harris Bilingual Elementary School), and Don McGrath (Chapter Chair).



Minh Quach of Agilent Technologies spoke to the Denver Chapter in April on signal integrity considerations and analysis, including a practical tutorial on high-speed test and measurement techniques (left to right): Bob Barnes (Treasurer), Tin Tin Wee (Secretary/Web master), Minh Quach, and Alvin Loke (Vice Chair).

Santa Clara Valley Chapter Report

Formation

In the fall of 1996 a colleague, Jonathan David, came into my office at Cadence Systems. He said the Solid-State Circuits Council would become a society next year and he thought a local SSSC chapter would be appropriate. I was involved in activities of other Santa Clara Valley IEEE chapters (Magnetics Society, Communications Society, and Microwave Theory and Technics Society). We discussed my experiences and I told him: "This is the place for an SSSC chapter." After 40 years, Santa Clara Valley is still the heart of the IC design industry.

The first meeting was scheduled shortly after the 1997 ISSCC. Ken Kundert, a Cadence Fellow and an expert in continuous time simulators, spoke on "Simulation of jitter in phase-locked loops using Spectre RF." Spectre is the continuous time simulator part of Cadence EDA suite tools. The inaugural meeting attendees signed the petition to form the chapter and Jonathan David became its first Chapter Chair.

The IEEE Executive Committee of the Santa Clara Valley Section advised that successful chapters operate with a fixed time and place for meetings to establish a regular attendance base. To avoid overlapping with other established chapters with similar technical interests,



Kris Pister lecturing on "Dust circuits and applications" at the 19 February 2004 technical meeting. The Santa Clara Valley SSSC Chapter meets the third Thursday of every month at the centrally located Cadence facility in a well-lit auditorium that seats 100, with two projectors and an amplifier system.

we picked the third Thursday of each month. We selected the centrally located Cadence campus as our meeting site. For over seven years we have held seven to nine technical meetings a year, recessing in July, August, and December, and sometimes in January.

The Events

We strive to serve our industry needs by having presentations on cutting-edge circuits, technologies, and methods, to advance the state of the industry, to broaden the knowledge of our members, and to provide networking opportunities for the speakers and attendees. Past presentation

topics have covered a broad range of circuits: from bandgap reference through RF power amplifiers, A/D converters, iterative decoders, filters, novel EDA tools, state-of-the-art microprocessors, and methods to achieve a 10-million-gate System On a Chip. We have touched exotic subjects like MEMS and even superconductor quantum phenomena in electronics. It has been our philosophy that a professional chapter should fulfill the professional needs of the members, rather than serve to reeducate with a lot of courses organized by university professors on university grounds. We let academia run those courses.

SOME HIGHLIGHTS FROM OUR PAST PRESENTATIONS.

6/15/00: "Mechanism of phase noise in the differential LC oscillators," Dr. Asad Abidi, UCLA

2/15/01: "Connecting to the optical network: Requirements and state of the art," Dr. Jeffrey Bostak, Vitesse Semiconductor

9/18/01: "Issues in phase-locked loop design for SOC applications," Dr. Joseph Ingino, Broadcom

10/18/01: "Analysis and simulation of PLLs for SOC applications," Dr. Bill Egan, Santa Clara University

3/15/01: "Wideband over-sampled data converters for wireless applica-

tions," Dr. Ali Tabatabaei, Stanford University's Integrated Circuits Laboratory

9/26/02: "Group delay in analog filters," Dr. Narendra Rao, Silicon Magnetic Systems

10/17/02: "Trends and challenges in multi-gigahertz microprocessor design" Mr. Stefan Rusu, Intel

11/21/02: "CMOS power amplifiers: Nonlinear, linear, and linearized," Dr. David Su, Atheros Communications. There were 89 attendees in the audience.

4/17/03: "Challenges in A/D design and practical understanding of their

specifications," Dr. Ion Opris (independent consultant). The number of attendees was a record 102!

8/21/03: "40-GHz OC-768 optical transponder in SiGe technology: CDR, 16:4 MUX and 4:1 MUX/CMU," Dr. Adrian Ong and Dr. Harry Tao, both from Big Bear Networks

9/08/03: "Challenges in achieving first silicon success for 10-Mgate SOC," Aurangzeb Khan, Cadence.

10/16/03: George Vendelin, professor at Santa Clara and San Jose State Universities, celebrated his induction as an IEEE Life Fellow (and his birthday!) by lecturing on "Lossless feedback

amplifier design." He was accompanied by more than ten of his university students, who enjoyed the contact with our chapter.

4/15/04: "A single-chip, dual-band, tri-mode CMOS transceiver for IEEE 802.11a/b/g wireless LAN," Dr. Masoud Zargari and Dr. Manolis Terrovitis, both from Atheros Communications

5/13/04: "The practice of analog IC design," Phillip E. Allen (lecturer), Schlumberger Professor School of Electrical and Computer Engineering, Georgia Institute of Technology

To determine events and speakers we use a variety of methods: consulting solid-state-related professional publications, reading industry trade magazines, surveying our attendees for suggestions and their interests, and reviewing ISSCC and CICC proceedings. It is a permanent task of every officer/volunteer to think about and suggest speakers at planning meetings, although we have tried a dedicated person, a program chair, to fulfill that task. Our speakers are experts and specialists from renowned companies in the industry, professors or PhD candidates from respected educational institutions, and IEEE Distinguished Lecturers. It takes a lot of energy and time to contact the speaker, to agree on the content of the presentation, and to have the speaker provide an abstract and a short biographical note, all of which will constitute the bulk of the scheduled meeting announcement.

While students are always welcome to attend, we make a special effort each year to invite presentations by PhD candidates from the local universities, primarily Stanford and U.C. Berkeley, to maintain a healthy level of communication between industry and academia.

Our chapter has grown to over 1600 members. Meeting attendees are mainly IC designers in the area. Most are IEEE members. Many Senior Members and numerous IEEE Fellows belong to our chapter, so we draw from a prestigious list of "Who's Who" in the field of solid-state circuits. Six to eight members become Senior Members every year. Our forum, through its meeting topics and the technical breadth of the presentations, is an incentive for attendees to become members of IEEE (if they are not yet).

In 2002 average attendance for three fall meetings was 77. For our nine meetings in 2003 average

attendance was 52. On May 13 this spring we broke all previous attendance records when 160 participants came to hear Phillip E. Allen, Schlumberger Professor School of Electrical and Computer Engineering from Georgia Institute of Technology, lecture on "The practice of analog IC design."



Santa Clara Valley Chapter officers (left to right): Web master Perry Chow, Chapter Chair Dan Oprica, Treasurer Eric Hoffman, Secretary June Song, and Host Jonathan David, the chapter founder. The Vice Chair, Sorin Spanoche, was absent for the photo.

Chapter Management

We meet on the Cadence Campus at 6:30 p.m. Refreshments are served and we network until 7:00 p.m., when the presentation starts. An hour to an hour and a half format is a more ample forum than compressed technical presentations at conferences such as ISSCC or CICC. Mostly we use a free format, allowing questions during the presentation, which makes the evening vivid, interactive, and more interesting. We allow time after the presentation for further discussions with the speaker, at his convenience. We present each speaker with a logo plaque as a gesture of our appreciation. At times, we invite the speaker out for dinner. We always ask the speakers to provide us with their presentation (in pdf or ppt format), which we post on our Web site with other interesting presentations (ewh.ieee.org/r6/scv/ssc).

The tasks of our elected officers are described in IEEE bylaws. We determined that, besides the four elected officers, three other volunteers are sufficient to run the chapter. It is essential to have an electronic communications person

(Web master) to maintain our RSVP email list and send periodic meeting announcements. The chapter host (a Cadence employee) arranges access to the meeting's premises. We would like to have a third volunteer, a hospitality chair, to organize publicity and order refreshments for the meetings. At the moment we take turns volunteering to fill that task. Most administrative matters are handled by email. Event planning is done at officers' meetings preceding or following the technical meetings and occasionally at other meetings that are called as needed.

A great help in publicity is the San Francisco Bay Area Council's electronic *Calendar & Newsletter* (www.ieee-sfbac.org/grid), where all our local chapter events are posted. Until April 2004 this was run by Doug Davolt (who recently retired), the editor of our local IEEE publication, *GRID*, for the last two decades. Paul Wesling, a seasoned Web master, now runs this local, web-only *GRID* publication.

If we had the time and budget, we would organize Short Courses and workshops, and assist with the ISSCC and CICC conferences in our local area. Last year we organized a course to help job seekers retrain themselves. We plan to have an RFIC design course for which I have drafted the contents. I need another three or more volunteers to accomplish this task.

Running a chapter, particularly one with numerous members, is a task of paramount importance. We are proud of our achievements and are very satisfied to serve our professional community. Organizing the events, meeting the speakers, and networking with our peers in an elevated professional environment, which we create, is a wonderful endeavor! ●

Dan Oprica

Santa Clara Valley Chapter Chair
oprivad@ieee.org

SSCS EVENTS CALENDAR

Also posted on www.sscs.org/meetings

SSCS SPONSORED MEETINGS

2004 CICC Custom Integrated Circuits Conference

www.ieee-cicc.org

3-6 October 2004

Caribe Royale Resort Suites, Orlando, FL, USA

Paper deadline: passed

Contact: Ms. Melissa Widerkehr,

cicc@his.com

2005 ISSCC International Solid-State Circuits Conference

www.isscc.org

6-10 February 2005

San Francisco Marriott Hotel, San Francisco, CA, USA

Paper deadline: 20 September 2004

Contact: Courtesy Associates,

ISSCC@courtesyassoc.com

2005 Symposium on VLSI Circuits

www.vlssymposium.org

16-18 June 2005

Kyoto, Japan

Paper deadline: 7 January 2005

Contact: Phyllis Mahoney,

vlsi@vlssymposium.org

or Business Center for Academic Societies Japan

vlssymp@bcasj.or.jp

SSCS PROVIDES TECHNICAL CO-SPONSORSHIP

2004 Asia-Pacific Conference on Advanced System Integrated Circuits (AP-ASIC)

www.ap-asic.org

4-5 August 2004

Fukuoka, Japan

Paper deadline: passed

2004 International Symposium on Low-Power Electronics and Design

www.islped.org

9-11 August 2004

Newport Beach, CA, USA

Paper deadline: passed

2004 Bipolar/BiCMOS Circuits and Technology Meeting

www.macs.ece.mcgill.ca/~rfic/bctm04/

12-14 Sept 2004

Montreal, QC, Canada

Paper deadline: 1 March 2004

2004 European Solid-State Circuits Conference

www.esscirc.org/

20-24 September 2004

Leuven, Belgium

Paper deadline: 22 March 2004

2004 Compound Semiconductor IC Symposium (Formerly IEEE GaAs IC Symposium)

www.csics.org

24 - 27 Oct 2004

Monterrey CA

Paper deadline: 3 May 2004

2004 International Conference on Computer Aided Design

www.iccad.org

7 - 11 Nov 2004

San Jose CA, USA

Paper deadline: passed

2005 International Conference on VLSI Design

www.isical.ac.in/~vlsi2005/

3-7 June 2005

Taj Bengal, Kolkata, India

Paper deadline: passed

2005 Radio Frequency Integrated Circuits Symposium

www.rfic2005.org

12-14 June 2005

Long Beach, CA, USA

Paper deadline: 3 January 2005

2005 Design Automation Conference

www.dac.com

13-17 June 2005

Anaheim, CA USA

Paper deadline: 22 November 2004

2005 Symposium on VLSI Technology

www.vlssymposium.org

14-16 June 2005

Kyoto, Japan

Paper deadline: 7 January 2005

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